UNIVERSITÄT DUISBURG ESSEN

Fachgebiet Hochfrequenztechnik

H F T

Fachbereich Ingenieurwissenschaften
Abteilung Elektrotechnik und Informationstechnik
Institut für Nachrichten- und Kommunikationstechnik

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Diplomarbeit / Masterarbeit

AUFGABE DER DIPLOMARBEIT
im Hauptstudium II

für: Herrn Milan Forcan

gestellt von: Herrn Prof. Dr.-Ing. K. Solbach
Fakultät für Ingenieurwissenschaften - Hochfrequenztechnik

Thema: **Concept Creation and Design of a Parameterizable, fast-locking 65 nm CMOS CDR-PLL for Gigabit Serial Chip-to-Chip Communication in Mobile Devices**

Description of Problem:
The work starts with the analysis of known concepts and latest publications to gain a comprehensive insight into state-of-the-art solutions for fast locking CDR-PLL's with a data rate in the 1.25 – 2.5 Gb/s range. Requirements and specifications of different standards will be extracted and summarized. Based on the result the target performance of the CDR-PLL will be defined, taking relevant system requirements into consideration.

The next step is to discuss and select most promising concepts and architectures to fulfil the defined characteristics. For these architectures appropriate models have to be developed for simulation and entered into the Cadence Design System database. From this first level simulation procedure, a final architecture selection has to be done.

The work will continue with schematic entry of the selected architecture, and detailed simulation. Hereby the generic engineering model (GEM) design methodology has to be applied. With the GEM approach, schematics, layout, simulation models, and testbenches are generated based on textual descriptions. Based on these descriptions the different views are generated using GEM command library and technology information.

After completion of the thesis work a public presentation of results is to be given at the department.