University Duisburg-Essen

The design and implement of power meter

For 7-Tesla MRI Power Amplifier

Bachelor Project

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Bachelor-Project Task

Power Meter for 7-Tesla MRI Power Amplifier

In a research project, the department develops a high pulse-power amplifier for a 7-Tesla Magnetic Resonance imaging (MRI) system. The power amplifier employs a high pulse-power final stage with a maximum of 1 kW output power into a 50 Ohm load at an operating frequency of 298MHz. Measurement of the power level and the amplitude envelope of the pulses is required during the assembly and matching optimization of the amplifier units.

The task is to design, build and test a power meter circuit on the basis of an envelope detector (integrated circuit log-amplifier AD8307) which provides a dc output voltage proportional to the logarithm of the input power level with a slope of 25mV per dB of RF input power. The input signal must be in the order of milliwatts so that only a sample of the 1 kW -pulse is to be fed to the IC. The main part of the power has to be absorbed in a 50 Ohm-load resistor which sits on a heat sink while a resistor-probe is used to take a sample of the high-power signal. The detector output voltage for our MRI power amplifier signals will show a pulsed dc level which is shifted by a bias voltage. In order to allow correct measurement of the pulse power level, the offset voltage has to be stripped off before applying the measurement. Measurement can be afforded by buffering the detector voltage and connecting it through a coaxial cable to an oscilloscope which will show the pulse envelope. As a built-in meter, an LCD voltage display module (e.g., Voltcraft DVM210) is to be included. This will require a sample & hold circuit (e.g., LF198) which is triggered by the TTL-pulse from the power amplifier control circuit (the so called "Un-blank" signal). When the sampling of the detector voltage is performed from shortly after the start of the power pulse to the end of the pulse duration, the voltage display can indicate correctly the instantaneous power level of the pulse.

In particular, the task entails the following steps:
- Design a circuit for the RF load, probe and the AD8307 plus the operational amplifiers required to cancel offset and as S/H-amplifier, buffer and scaling circuits for the output voltages. Examples for various parts of the circuit are available from other projects and from manufacturer data sheets. Design a circuit to provide variable delay to the trigger voltage allowing to move the sampling instance along the pulse duration of up to 5 msec.
- Design a PCB using EAGLE software
- Assemble the circuit after production of the PCB at our workshop.
- Test the circuit regarding impedance match, insertion loss of the probe and the output voltage of the IC; the circuit should function over 10 MHz to 50oMHz but should be Optimum at 298MHz.
- Adjust the output voltage of the circuit and set the LCD voltage display module such that at 1kW pulse power the display shows a numerical value of 60.0, representing 60 dBm power. This can be adjusted using low-power signals from a test generator with precise output levels in the milliwatts range.

- Compare the results of the power meter display with measurements using an oscilloscope.
- Verify the proper functioning of the circuits using a signal from a high-power amplifier with CW- and pulsed excitation.
- At the end of the work, a public presentation of results is to be given.

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1. Requirements Analysis

A power meter needs to be designed with following requirements:

- Input pulsed RF signal with maximum power 1kW.
- Output the power numerical value with the unit dBm.
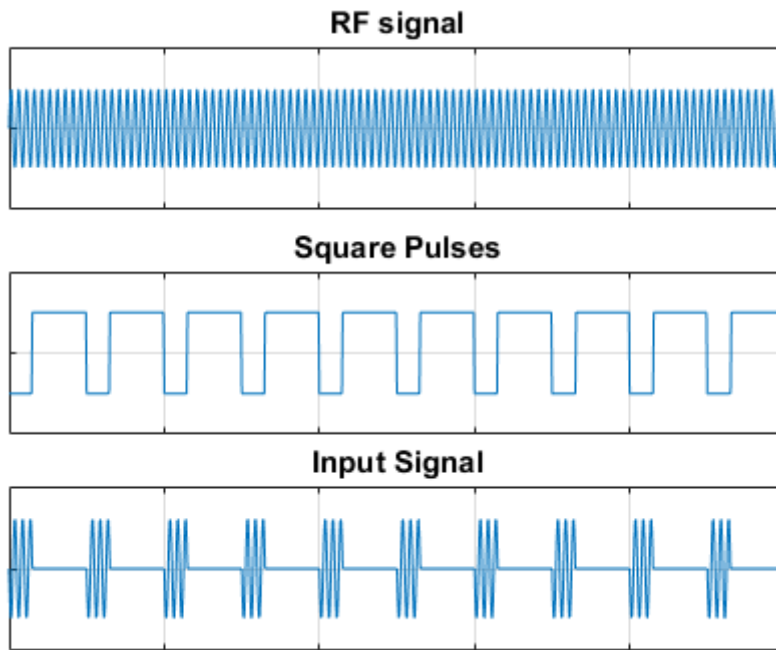- System should be optimum at 300MHz

Fig.1 Input signal

- Chip AD8307 and LF398 should be used in the circuit for signal conversion and sampling.
- LCD module DVM210 should be used for the result display.

The power meter is feed with the pulsed RF signal, after process the power value of the signal should be displayed on the LCD.
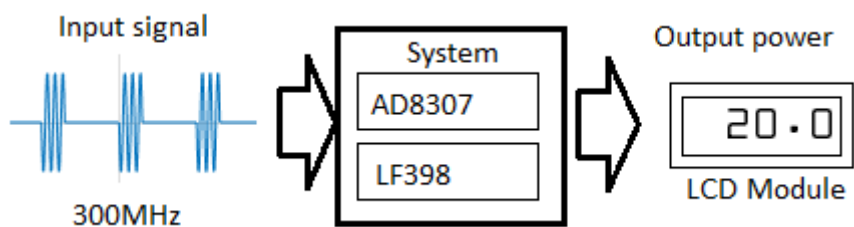

Fig.2 System flow

2. System kernel model construction

Before the circuit design, the system model should be built. The model consists of four parts and is shown as follow:
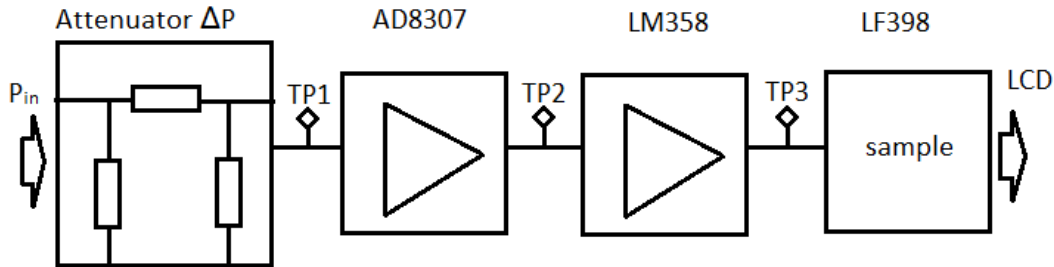

Fig.3 System model

2.1 Power attenuator
The input of the attenuator is the system input P_{in}.
The output of the attenuator is the test point TP1.
The value of attenuator coefficient is ΔP. The theoretic value is 60dB.

$$\text{TP1} = P_{in} - \Delta P \tag{1}$$

2.2 Chip AD8307
The function of AD8307 is transferring the power difference to a small voltage level. The transfer factor is 25mV/dB.

If there is no input, the chip has a small output voltage U_0. The result of U_0 measuring is about 0.2V. In real condition, the low part of the output curve is not linear.

The power difference is the subtraction of input power and initial power P_0. The initial power P_0 can be found in the data sheet. (P_0 = -80dBm)

The output of the chip is TP2.

$$TP2 = U_0 + (\text{TP1} - P_0) \cdot 25\text{mV/dB} \tag{2}$$

With (1),

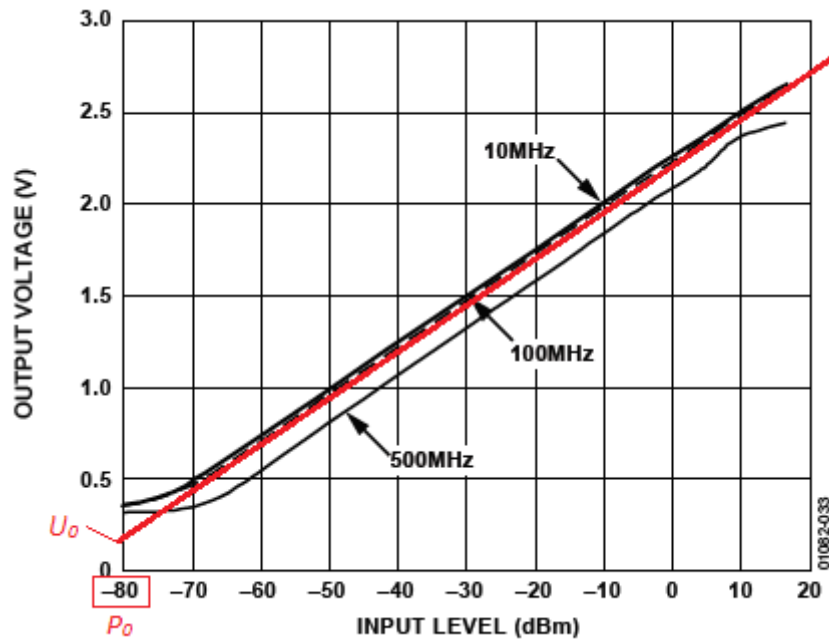$$TP2 = U_0 + [(P_{in} - \Delta P) - P_0] \cdot 25\text{mV/dB} \tag{3}$$

Fig.4 Input / Output curve of AD8307

2.3 Operational Amplifier LM358

The function of Op Amp is transferring the AD8307 output voltage value to the final power value in voltage form. This function controlled by a group fix value resistor and a variable resistor. The formula form of the circuit function is as following:

$$(U_1 - U_2) \cdot R_{ratio} \tag{4}$$

The output value of this part is TP3.

The calculation actually is the inverted of the formula (3). TP3 equals to P_{in}.

$$TP3 = P_{in} = \frac{(TP2 - U_0)}{25mV} + P_0 + \Delta P \tag{5}$$

In order to fit the form of (4), formula (5) should be reformed as follow:

$$TP3 = \frac{TP2 - U_0 + 25mV * P_0 + 25mV * \Delta P}{25mV} \tag{6}$$

In formula (5) and (6), P_0 and ΔP no longer have the meaning of power. They become the voltage level. Only the magnitude equals to the value of the power.

2.4 Sample chip LF398

The sample chip LF398 gets the value of TP3 and outputs to the LCD module.

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3. Implement of modules

Based on the system model, the respective circuit of modules can be designed.

3.1 Attenuator
From the datasheet of the AD8307, the max linear input power is about 10dbm. But for real requirement, the maximal input signal is 1kV. Thus an attenuation circuit is necessary.
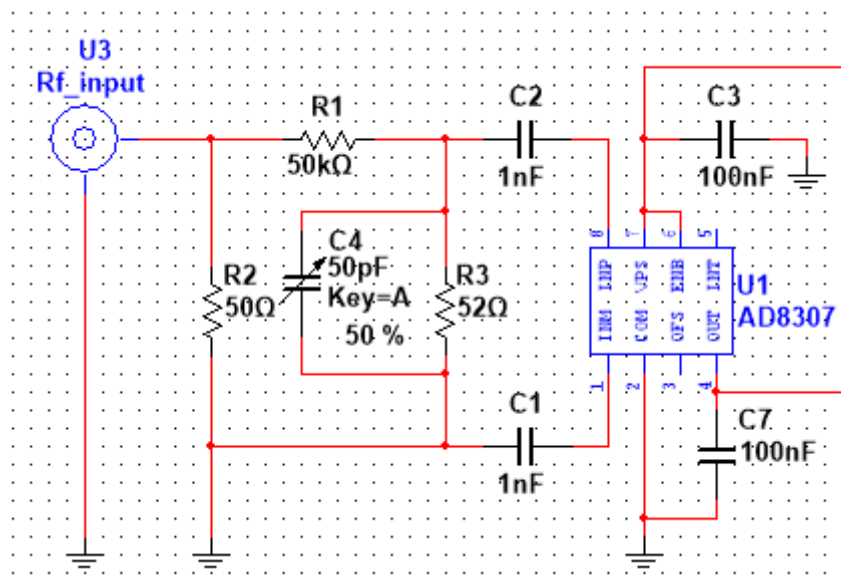
A. Base circuit
The π-circuit is applied here.

Fig.5 π-circuit networks

R_2 is a power resistor which value is 50Ω, 50W. This resistor used to absorb the power from input.

R_3 is a matched resistor for AD8307 and value is about 52Ω.

Value of R_1 needs to be estimated.

V_{input} = 1000V, the equivalent voltage value of 10dbm is 1V.

R_2, R_3 full fill the relationship of voltage divider.

$$\frac{R_3}{R_3+R_1} = \frac{1V}{1000V} \Rightarrow R_1 = 50k\Omega \tag{7}$$

The base circuit is determined here.

B. High frequencies behaviors
The input signal will be 300MHz. Thus the value of resistor of R_2, R_3 will be change.
The compensation should be applied in the circuit.

The SMD resistor will be used in real circuit. A simple model is built to analysis the condition in High frequencies.
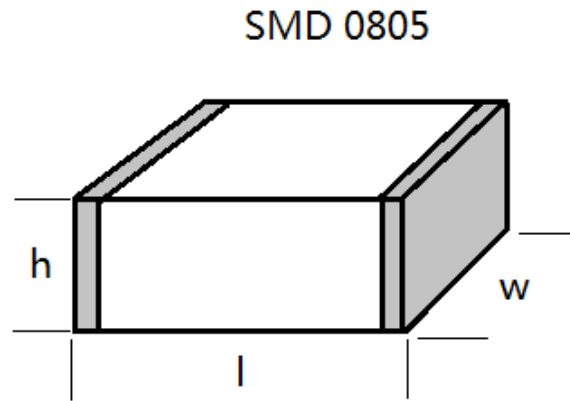
4

Fig.6 the SMD resistor

The size of SMD l=2mm, h=0.5mm w=1.2mm. The permittivity of material ε_r is about 10.

The resistor is treated as a parallel plant capacitor. The capacitance value could be estimated by formula:

$$C_p = \varepsilon_0 \varepsilon_r \frac{wh}{l} \qquad (8)$$

The result C_p is about 0.03pF.

Then the software Qucs is applied to simulate the condition of R_1, R_3 parallel with C_p in 300MHz.

a) **The value change of R_2=50kΩ in High Frequencies.**
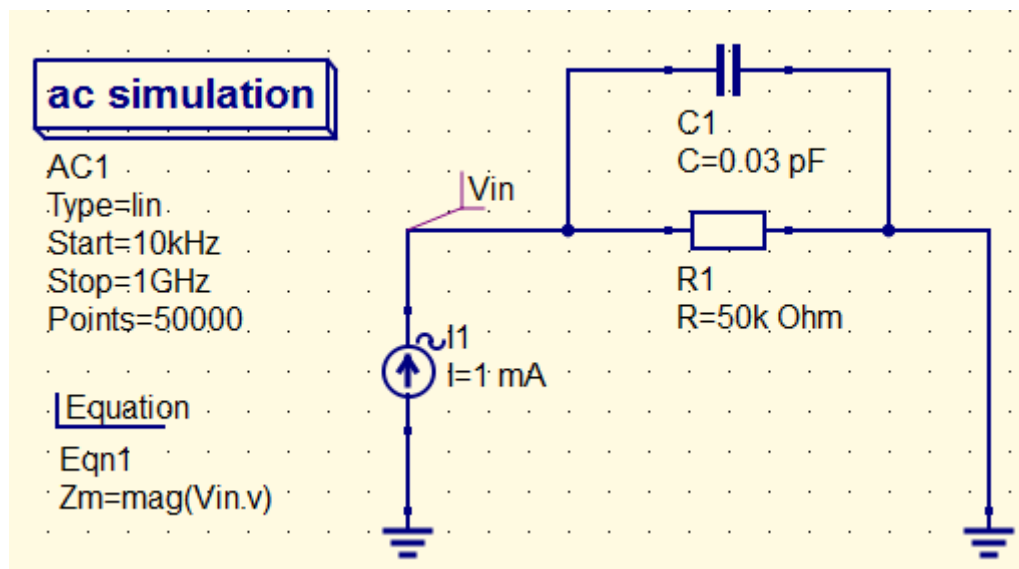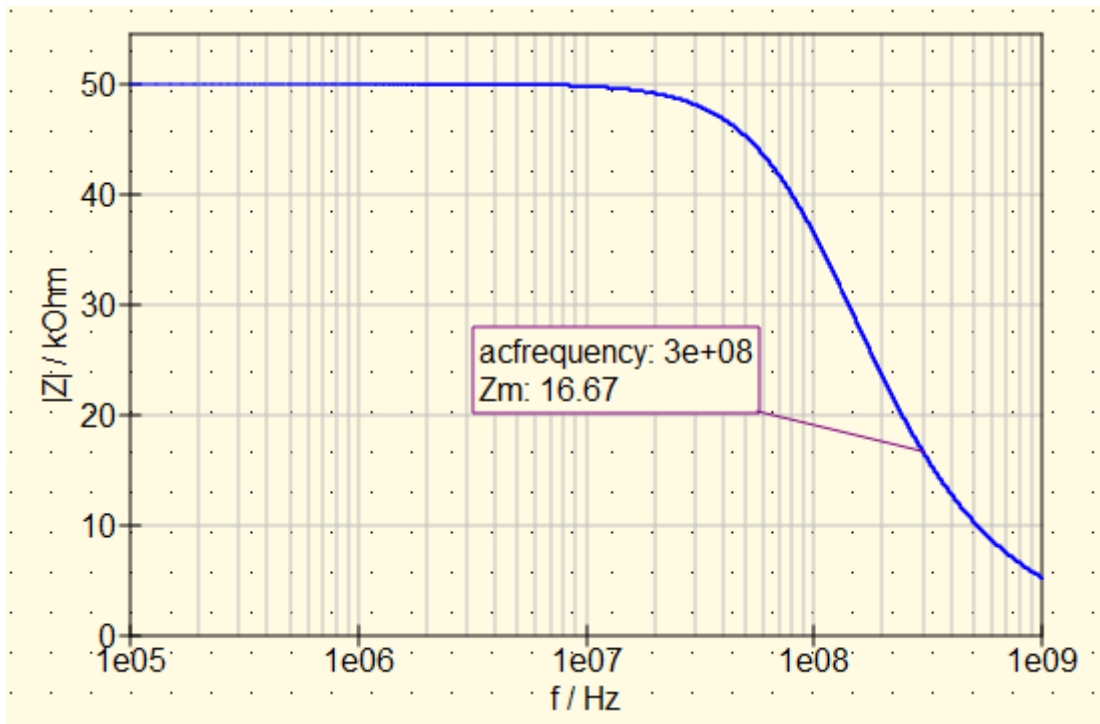

Fig.7a. HF simulation of R_2

Fig.7b HF simulation of R_2

From simulation, the Impedance of R_1 will decrease in 300MHz, the value becomes to 16.67kΩ. Thus the ratio of the voltage divider will be change.

b) The compensation capacitor value estimated by simulator.

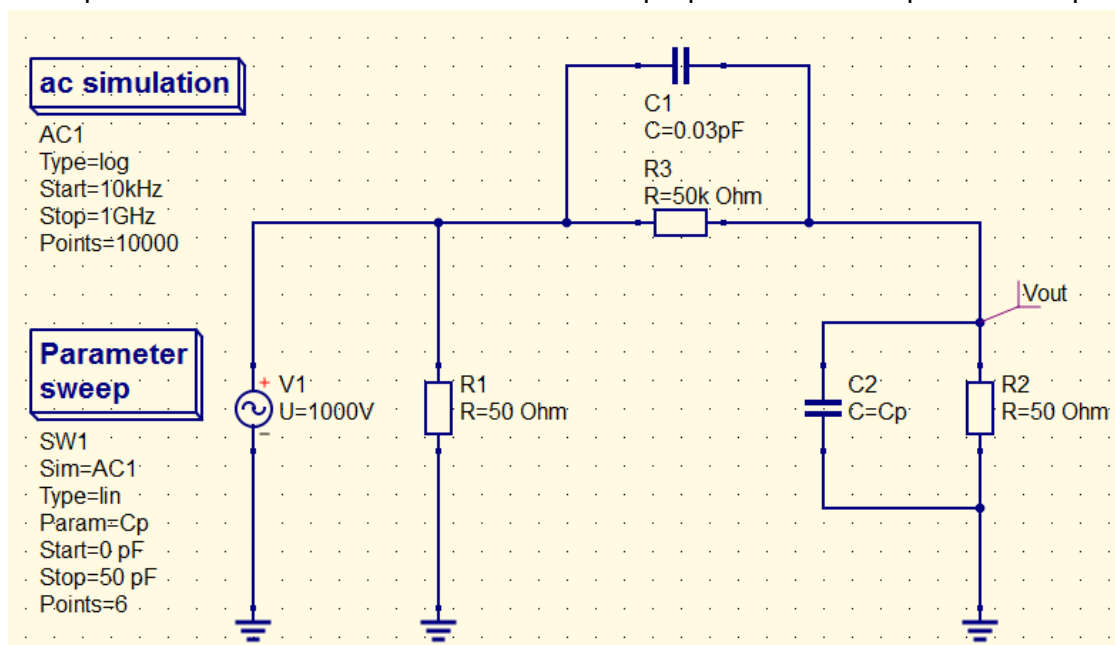The complete attenuation circuit is built to find the proper value of compensation capacitor.

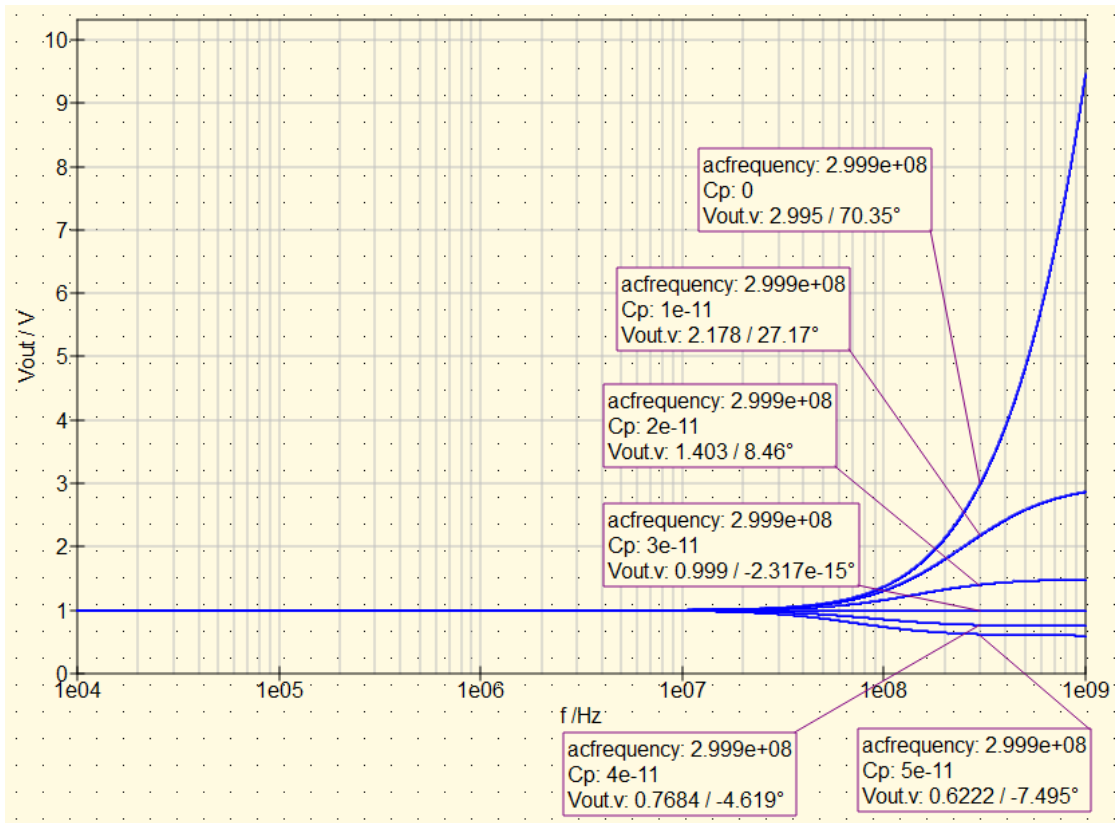Fig.8a Simulation of compensation capacitor

Fig.8b Result of simulation with compensation capacitor

The value is between 20pF to 50pF. In real circuit, a variable capacitor will be used to get a proper value.

3.2 Analog signal conversion

After attenuator, the signal is processed by chip AD8307. Then a convert circuit which can transfer the output voltage of AD8307 in to the final result in numerical needs to be design. The operation amplifier LM358 is used to achieve the purpose.

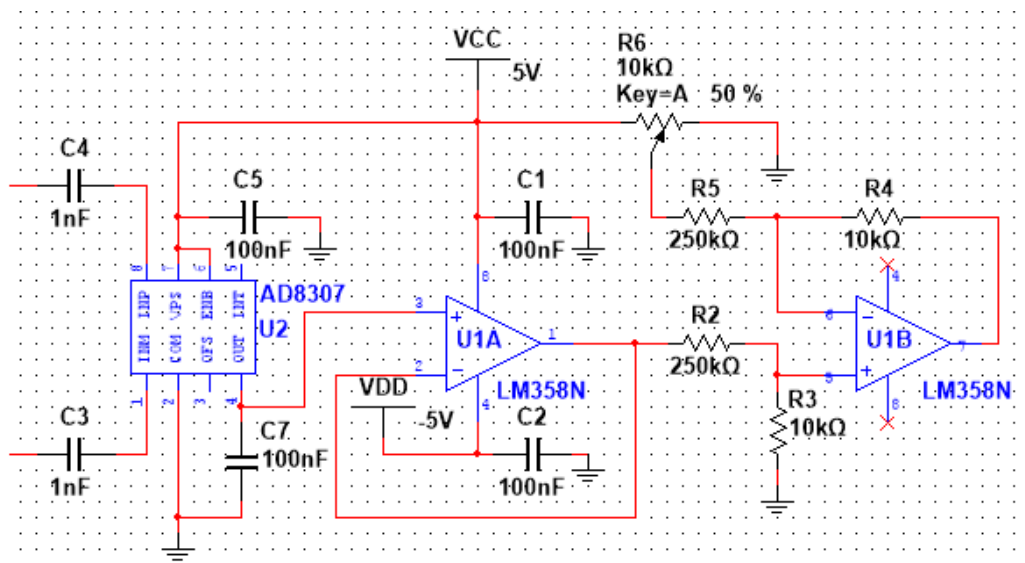The circuit is shown as follow:

Fig.9 Analog signal convert circuit

U1A is the one of amplifier units in the LM358. It is used as the voltage follower.

U1B is the second amplifier units of the LM 358. It is used as a differential circuit to transfer the output of AD8307 to the final result. (The DVM module has the range -200mv to +200mv.)

In the circuit, R2 = R5 and R3 = R4.
R5/R4 = 25, this value is same with the output characteristic of the AD8307, which output slope is 25mV/dBm.

Then the output of U1B (pin7) can be calculated by follow equation:

$$U_{pin7} = (U_{pin5} - U_{pin6})\frac{R_4}{R_5}$$ (9)

This equation is match with the equation (4) in the system model. U_{pin5} is the output of U1A, actually is the output of the AD8307. U_{pin6} is the reference potential. Based on the system model, this value can be applied for calibration and zero point adjustment.

Fig.10 the output example

Fig.10 shows the example in real circuit. The red line is the output in the test point. Left picture is the output of AD8307. With the processing of convert circuit, the output curve is shifted and compressed into the form in the right picture.

3.3 Sample with the TTL signal
After processing by convert circuit, the voltages cannot be displayed on the DVM module. The result should be sampled

Basic Sample circuit
According to the specifications of the LF398, when pin8 is given a high voltage TTL signal which is greater than 5V, the chip works under "sample state", the output will follow the input.

The hold capacitor C5 will keep the sample value in a short time after the pin8 switch back to 0V.

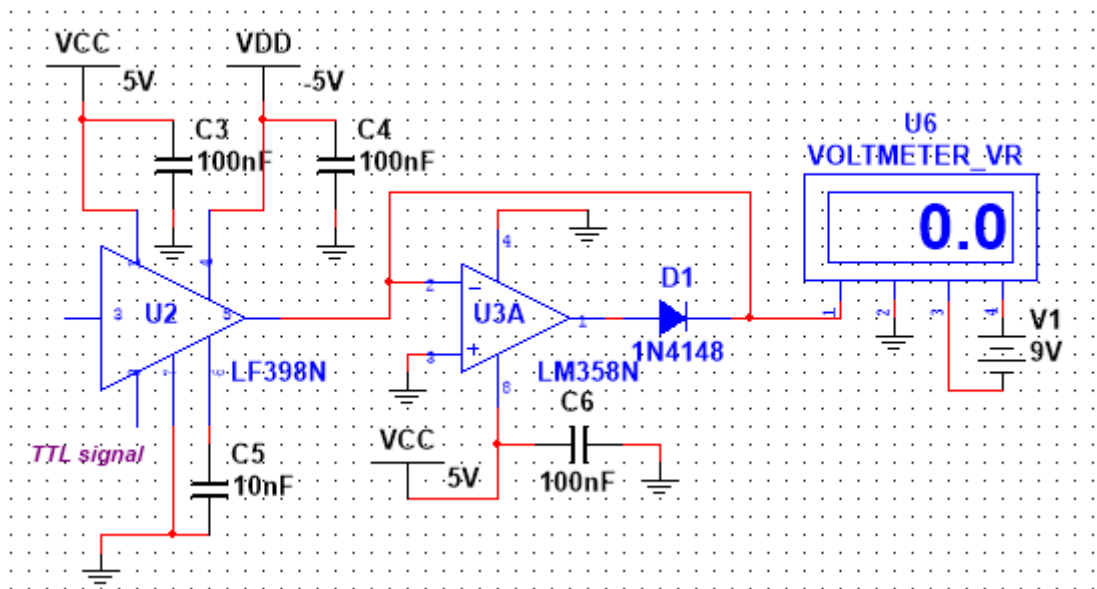Then the sample value will fall down to a very low (negative) power level.

Fig.11 Basic sample circuit

Between the output of LF398 and DVM, there is so-called "precision rectifier" circuit. The function is similar as a diode, which can keep the circuit above 0 voltage level. It consists of an amplifier and a diode. One unit of LM358 is used to implement this function.

Sample wide adjustable circuit
The basic sample circuit only work with fixed width TTL signal. In order to get different section of the output curve. The width of TTL signal should be variable and adjustable.
The 555 Timer will be used to change the width of the TTL signal.

Basic function of chip NE555
The 555 Timer has many different work mod. Here, only the mono stable operation will be discuss. The circuit and the waveform shown in follow:
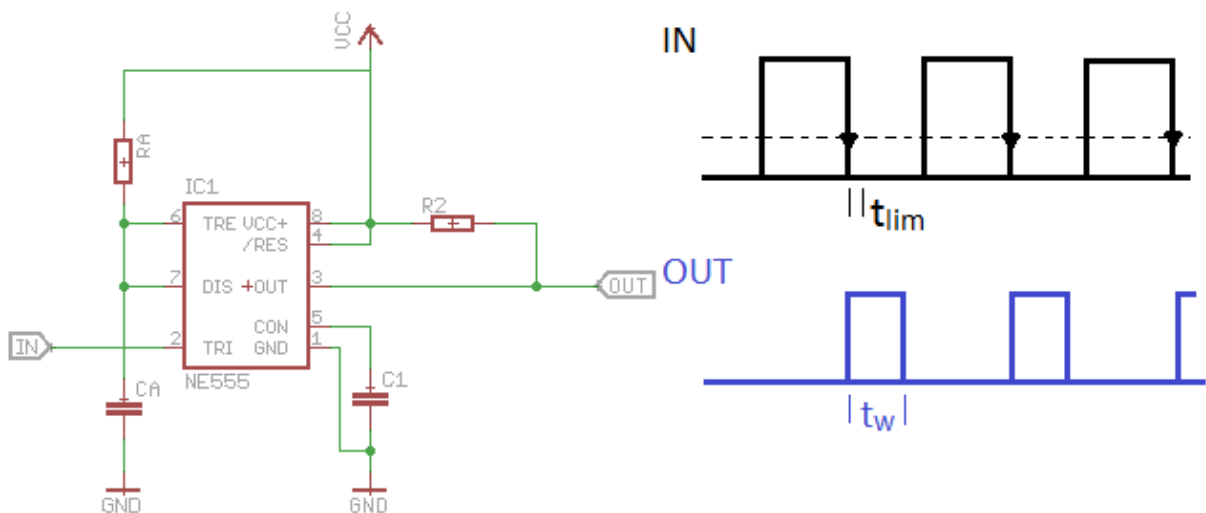

Fig.12 The mono stable circuit and waveform of 555

In circuit the pin 2 is feed the control TTL signal, every time when the TTL falling to 1/3 of its full high, the output will be trigged and creates a high level pulse signal. The duration of the output pulse is controlled by Ra and Ca.

$$t_w = 1.1 R_a C_a \qquad (10)$$

The 555 has a minimal response time t_{lim}= *10us* when the input signal reaches the trigger point.

The circuit should be modified to fit the design goal. The output duration time should be variable.

The phase of output should be same with input TTL signal.

The improved circuit
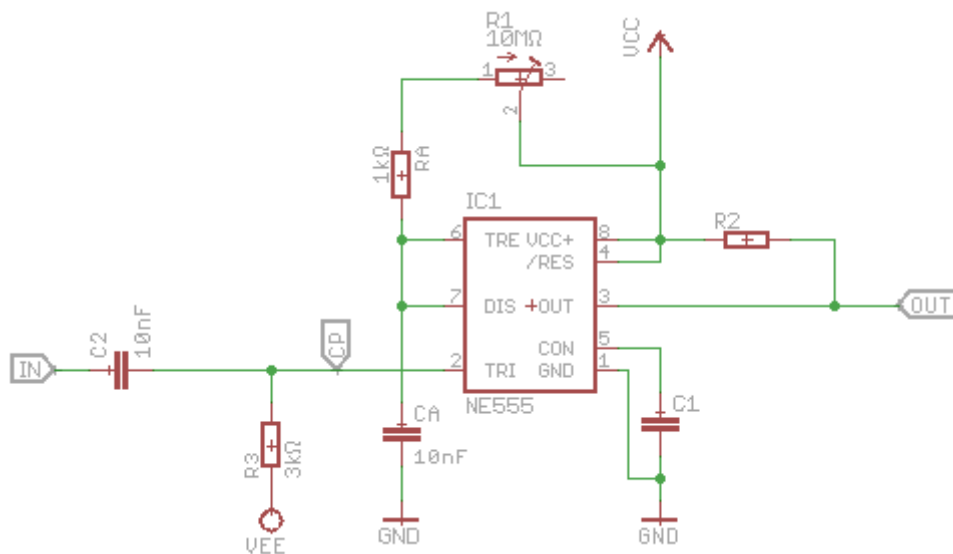
The improved circuits shown as follow:

Fig.13 The improved circuit

For the variable duration, a variable resistor R_1 added to the circuit. The max value of the resistor is the 1M ohm. The capacitor C_a uses the fix value of 10nF.

Thus the min and max duration can be calculated.

$$t_{w,min} = 1.1 R_a C_a = 1k\Omega \times 10nF = 1 \times 10^{-5} s \qquad (11)$$
$$t_{w,max} = 1.1 R_1 C_a = 10M\Omega \times 10nF = 0.1s \qquad (12)$$

For the phase synchronous, a proximate method is attempted.

The RC differential circuit is used as the peak detector. R_3 and C_2 are added in the circuit.

RC peak detector checks the rising of the input TTL signal, and transforms the wave form rectangle to very sharp pulse (result in CP point). The Fig.14 shows the process.
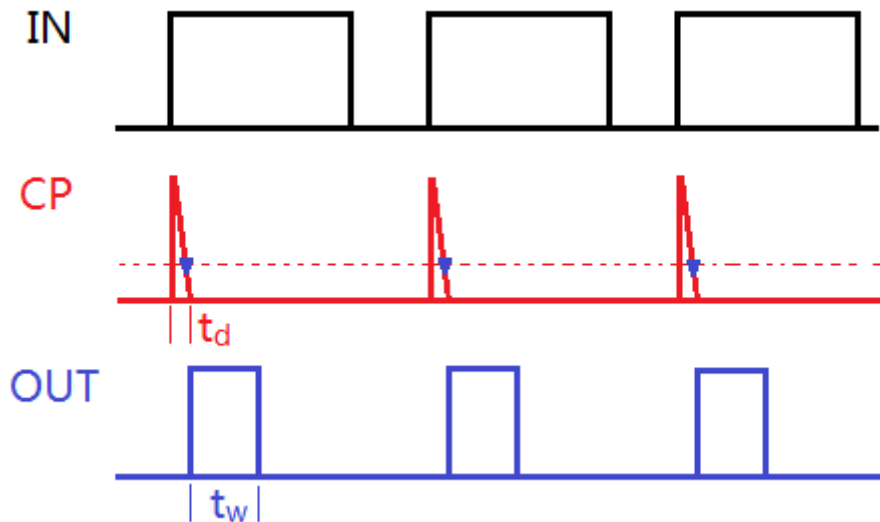
Fig.14 Work flow of circuit

Then the chip 555 receives the sharp pulse and trigged at the falling position. It produces the output waveform which has nearly same phase with the input TTL circuit.

The minimal duration t_d of sharp pulse should as small as possible in theory. The capacitor C_2 in RC differential circuit uses fix value 10nF and the proper value of R_3 is about 3kΩ after test in Lab.
Thus the small time delay t_d before 555 trigged can be estimated.

$$t_d = R_3 C_2 = 3k\Omega \times 10nF = 3 \times 10^{-5}s \qquad (13)$$

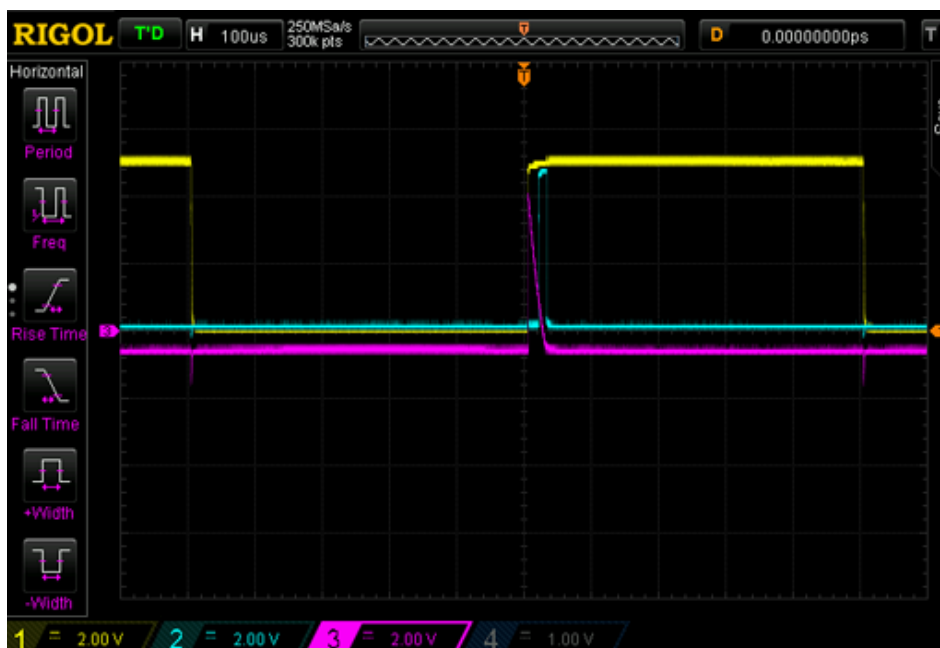These also the real waveform in test and show in follow:

Fig.15 Use RC circuit as peak detector

Fig.15 shows the RC circuit produces a sharp pulse (red) at the rising of TLL signal (yellow). At this time, the 555 produce the output with Ra in minimal value.

The next picture shows that 555 produce the output with Ra in greater value. Left is Ra in minimal value and right is Ra in greater value.

Fig.16 Different output with changing the Ra

3.4 main board circuit

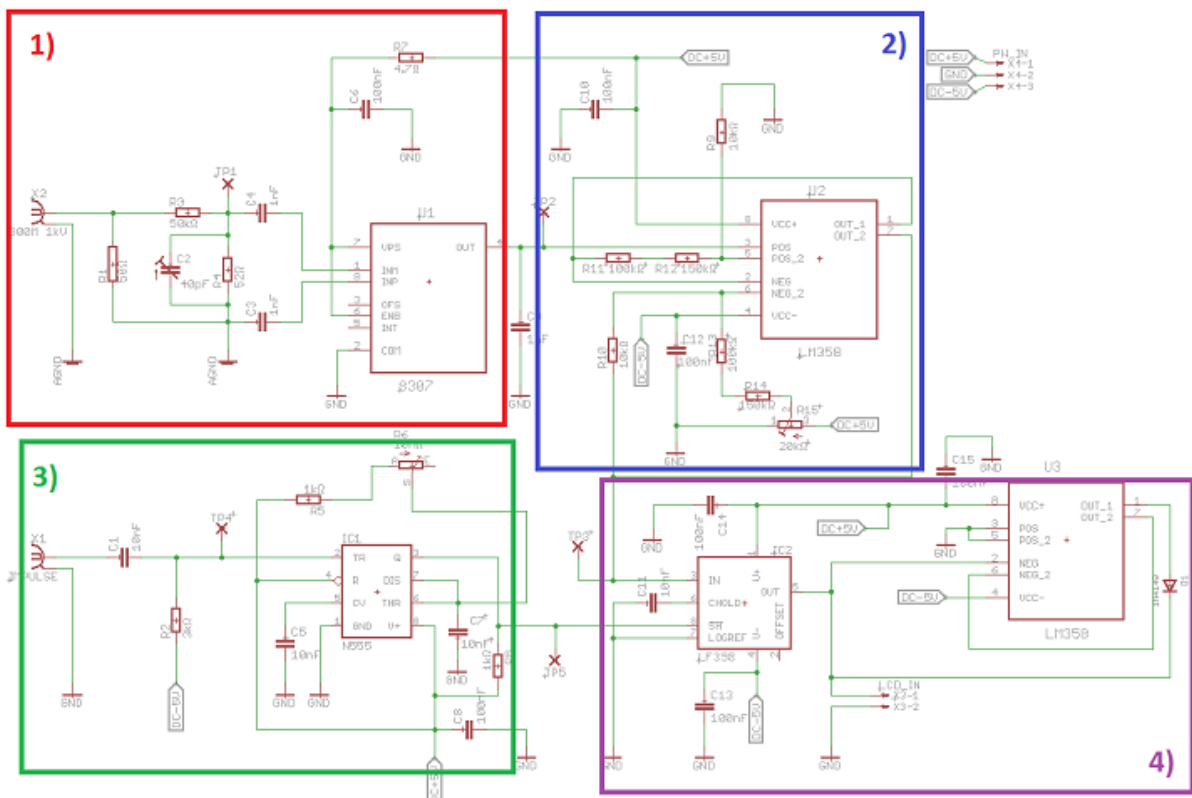4 units above constitute the main board.

Fig17. Main module circuit

1) High frequencies unit (AD8307).
2) Zero point adjusting and signal transform (LM358).
3) TTL processing (NE555).
4) Sample and hold (LF398 and LM358).

3.5 Power module

In system, every chip has different power supply requirement. Thus an individual power supply circuit is necessary.

Requirement of system (data from datasheet)

Chips	Number	Voltage /V
LM358	2 pics	±1.5 to ±16
LF398	1 pic	±3.5 to ±18
NE555	1 pic	4.5 to 16
AD8307	1 pic	2.7 to 5.5
DVM (LCD)*	1 pic	9V

The DVM should use the individual power supply. An individual 9V battery is used for DVM in real circuit.

The V_{min} = 4.5V and V_{max} = 5.5V of the power supply were restricted by chips NE555 and AD8307. Based data above, new power supply design as below:
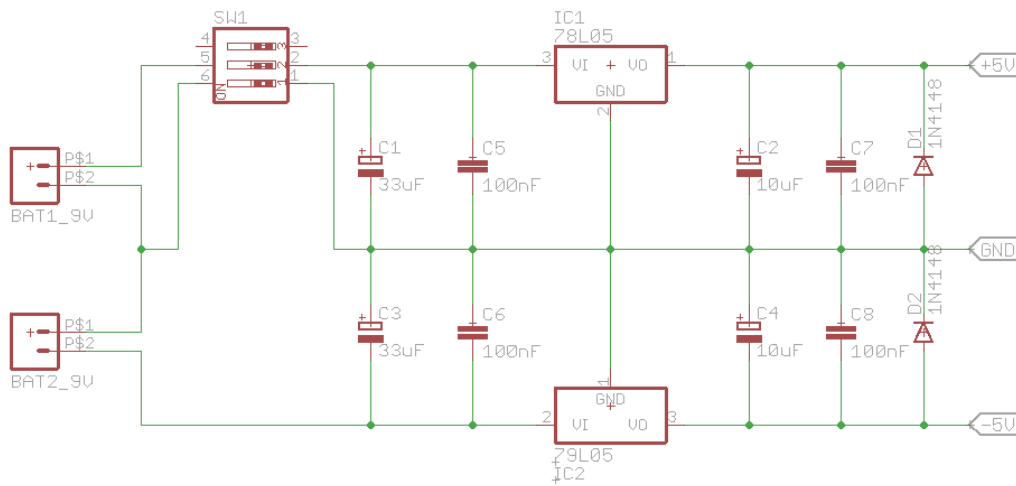

Fig.18 power supply

Two 9V batteries are applied as main power. In order to get the ±5V voltage, the voltage regulator chip 78L05 and 79L05 are used.

3.6 LCD module

According the datasheet of DVM, the module has "Hold" and background light function.
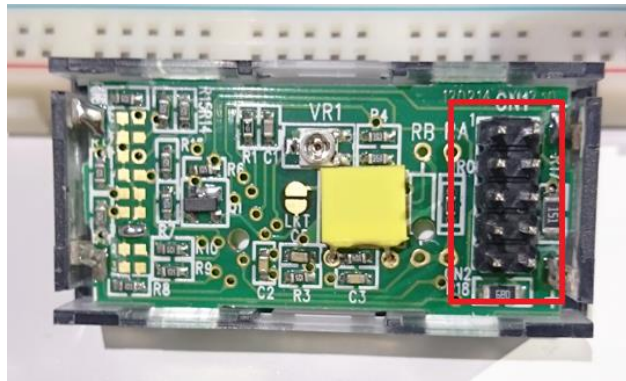At backside of the DVM, there are 2 columns 10 pins interface.

Fig.19 Backside of DVM

Pin 1, 2 are measurement probe.
Pin 3, 4 are 9V power input.
Pin 5, 6 If connected, the background light will be lighted up. The jump pin CN2 (pin9, 10) should be connected.
If Pin7 connects to Pin3, the figures shown on the DVM will be "Hold".

Based on the info above, the simple circuit designed to implement these functions.
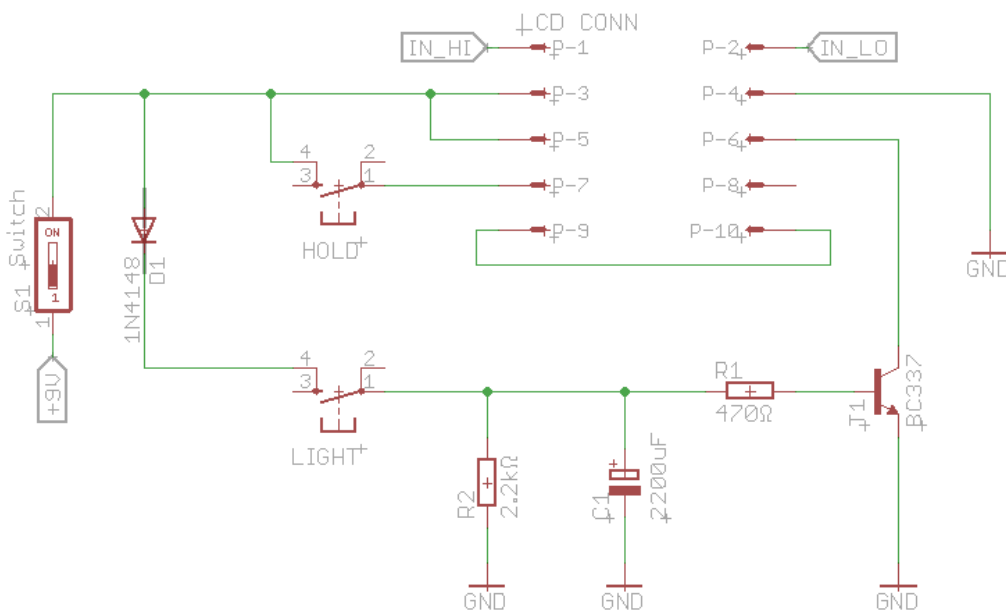

Fig.20 DVM circuit

In the circuit, between Pin 7 and Pin 3, a button is set to run the Hold function.

Between Pin 5 and Pin 6, there is a simple time delay circuit. After man release the button, the background light will keep about 3 seconds then go out gradually.

The basic principle of this time delay circuit.
Transistor T_1 play a role of switch. When the button is push down, all the circuit turns on. The capacitor is charged in a short time and the background light begins work. After the

button release, the capacitor discharge in a long time. Current go on flowing to T_1 and keep T_1 working till the discharge finish. Then T_1 turns off, therefore the background light loop is also cut off.

The different capacitor value can be change to get different delay time. Here the 2200uF is used.

4. PCB design

The software EAGLE is applied to design the PCB for 3 modules.

4.1 Software configuration

After setup the software, the component library should be added.

Extra library can be downloaded from follow website:

https://www.element14.com/community/community/cadsoft_eagle/eagle_cad libraries

+ Vishay
+ Texas Instruments
+ ST Microelectronics
+ Analog Devices
+ Linear Technology

https://github.com/rodan/Simplex-Eagle-Libraries

https://github.com/sparkfun/SparkFun-Eagle-Libraries

Decompress the download file, copy the ".lbr" files to the EAGLE installed path /lbr folder.

4.2 Basic step of PCB design with EAGLE

A. Draw the circuit schematic

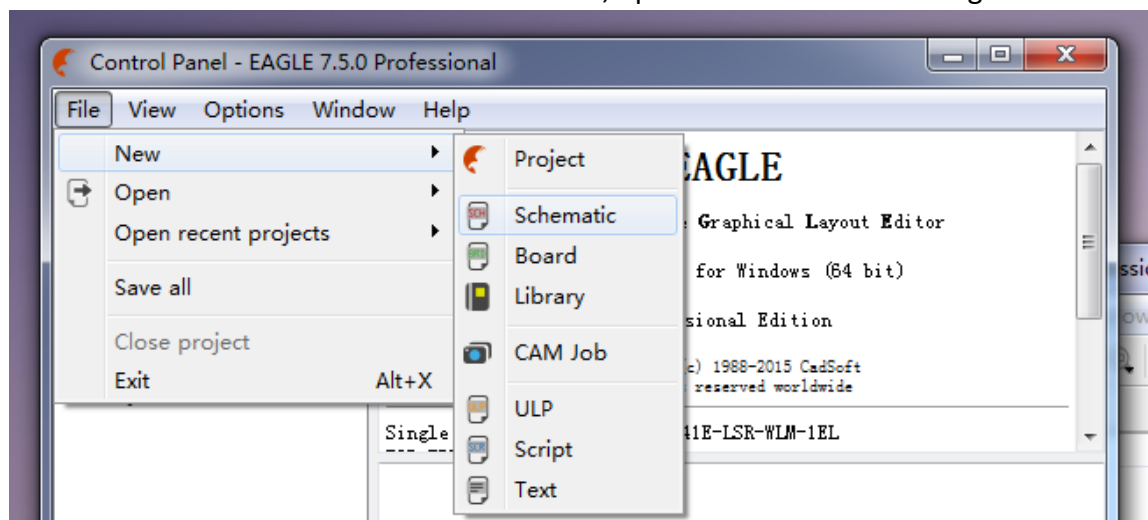1) From the menu "File" -> "New"->"Schematic", open a new schematic design window.

Fig.21 New Schematic window

2) Grid setting. From menu "View"->"Grid", open the "Grid" setting windows. Usually the grid display sets to "on", size sets to 50mil.
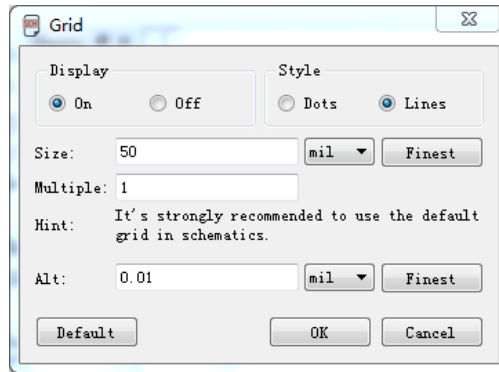
Fig.22 Grid setting

3) Add components to draw the circuit schematic. From menu "Edit"->"Add", open the "Add" windows. Input the key word to find the component, add it to the work area. In this window, the package info of the component also is shown.
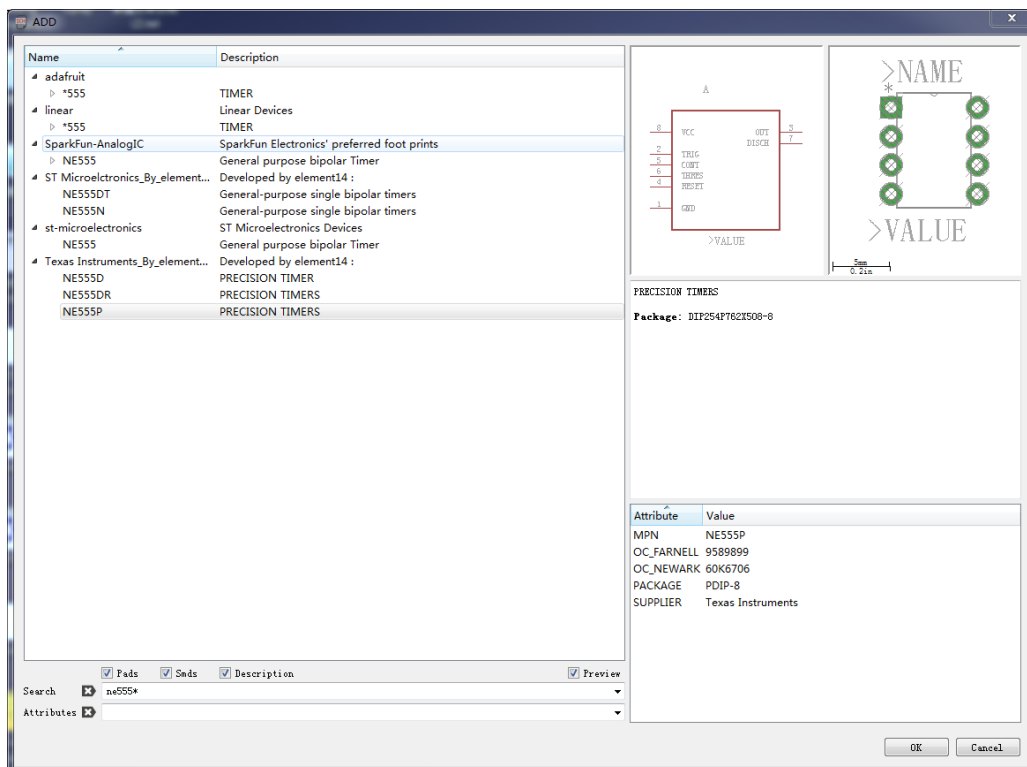

Fig.23 Add component

4) Commonly used draw tools
   These tools can be found on the left side of the window or in the menu "Edit" and "Draw"

Icon	functions
	Show the component detail information. In the menu "View" -> " Info"

	Move the components.
	Rotate components.
	Change the graphic attribute of the component. E.g. Align, Fonts, Size, and Layer etc.
	Delete component.
	Component Name setting
	Component Value setting
	"Smash" Separate the Name/Value from component symbol
	Draw the connection wire
	Add text to the symbol
	Add junction to the wire cross
	Add label to the connection wire

5) When finish the schematic drawing, do the electric rule check (ERC). From menu "Tool"-> "ERC". After checking a window will show the check result and detail error information.

B. Design the board

1) The circuit schematic should transform to the board design. From the menu "File"->"Switch to board". The board window is opened. All the components lie on the side of work area. The components are connected with yellow line which is called "air wire".
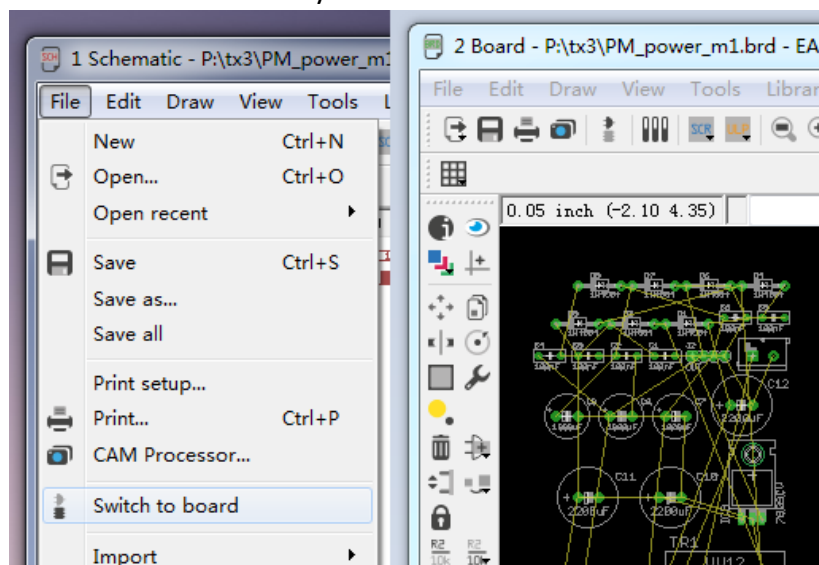
Fig.24 Switch to the board mod

Point to attention: Do not close the schematic window, both windows are binding and if the design changes in schematic, the board window will also change respectively.

2) Drag the components to the proper position in the board rectangle (gray line rectangle) on the work area. After laying the components, the tool "Ratsnest"() can arrange the air wire again to fit the new position.

3) Define the "net classes", From the menu "Edit"->"Net classes…", open the "Net classes" window and fill with proper values for the line width, drill and tolerance. The different line type also can be defined here. This function will be used later.
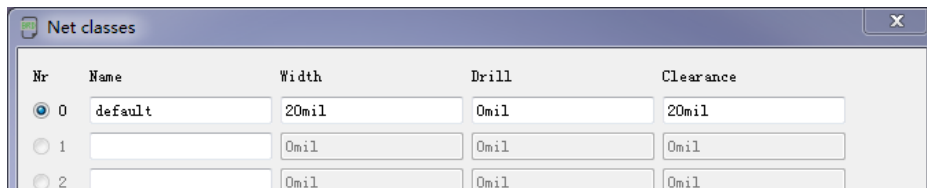
Fig.25 Net classes define

4) Define the "Design Rule Check (DRC)". DRC is the layout rule. From menu "Tools"->"DRC", open the DRC define window. Set the proper value for the PCB element attribute.
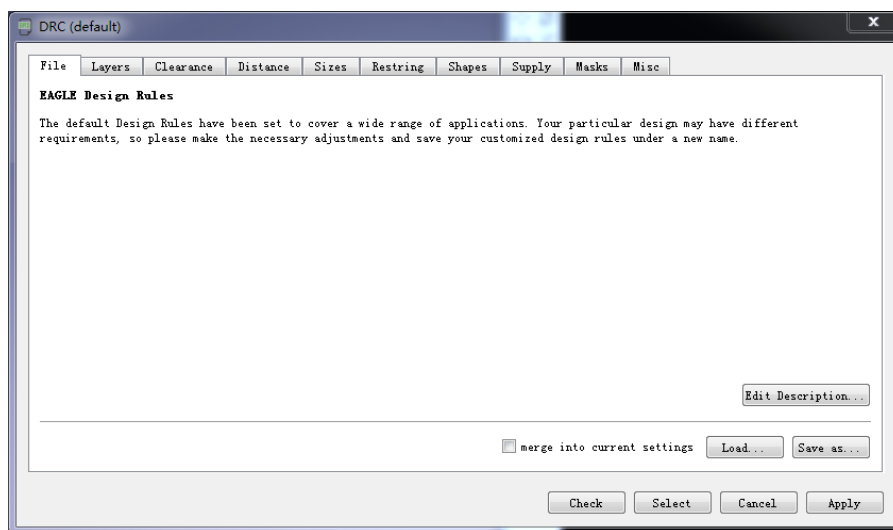
Fig.26 Design Rule Check

5) Use the "Autorouter" tool to draw the wire on the board. From menu "Tools"->"Autorouter", open the "Autorouter" window. Select the wire direction on the left and grid dependency rule on the right. Then the software can give a layout solution for the circuit schematic.
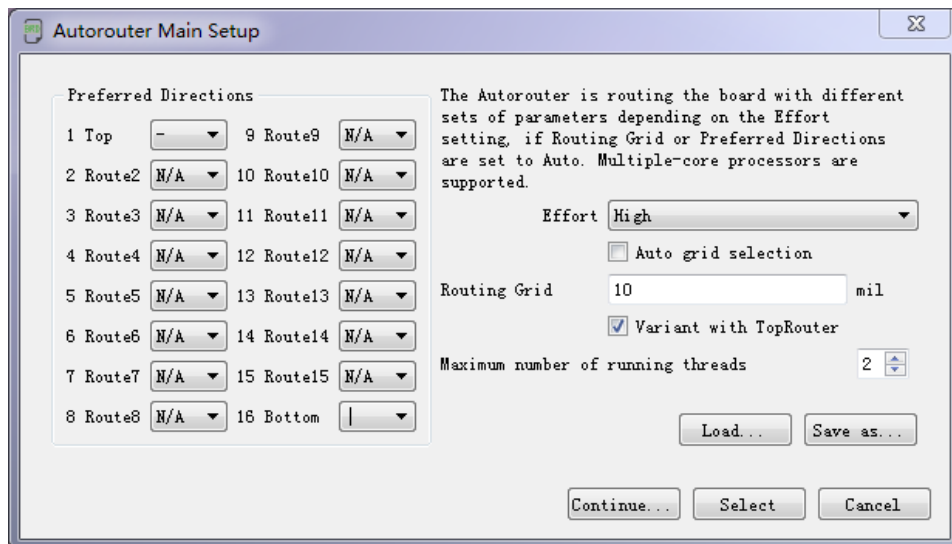
Fig.27 Autorouter

6) Or the manually draw the wire by using "route" tool ( ). When use the "route" tool, the wire attributes can be selected on the top of work area. E.g. The layer of the wire, the wire bending type, wire width, via type etc.
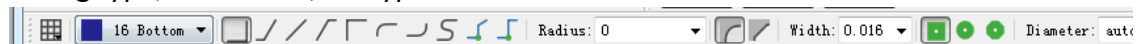
Fig.28 wire attributes

If wire layout is needed to cancel, use the "ripup" tool ( ). This operation does not cut off the real connection (the air wire is keeping), just delete the wire lays on the board.

7) After the layout design, run the DRC to check if any error exists in the design.

C. The special points about project PCB design.
According the steps which are introduced in section 6.2, the PCB design can be almost finished. There are still some different points which are needed to explanation.

a) About layer
Different PCB elements are on the different layer. In EAGLE, layer can be setting in menu "View"->"layer setting". In this window, all the possible layers are shown with different identify colors. The layer visible or add/delete operation can be done here.
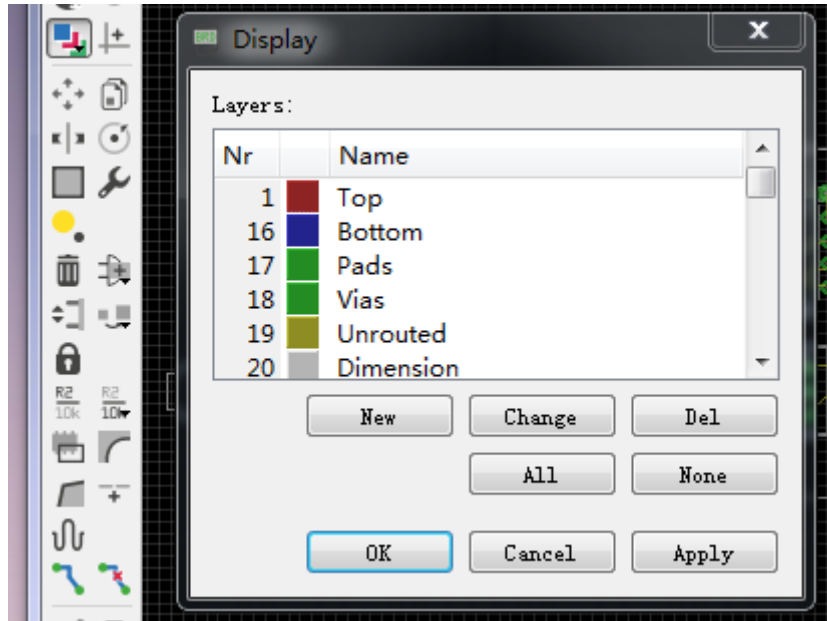
Fig.29 Layer setting

Following tables are some commonly used default layer.

Num.	Name	Description
1	top	Top side of PCB. Most components and wires lay on this layer.
16	Bottom	Back side of PCB. Few components and wires lay on this layer.
17	Pads	Solder Pads hole
18	Vias	Conductor holes though the PCB
21	tPlace	Silk screen, top side, For the short text
22	bPlace	Silk screen, back side, For the short text
25	tNames	Text of component names at top side
26	bNames	Text of component names at back side
27	tValues	Text of component values at top side
28	bValues	Text of component names at back side

b) General DRC setting

These DRC settings are used for all there module (power supply, DVM, main)

 The board dick is 1mm, both side has copper layer with 18um dick. These values should be filled in to "DRC" ->"layer" panel.
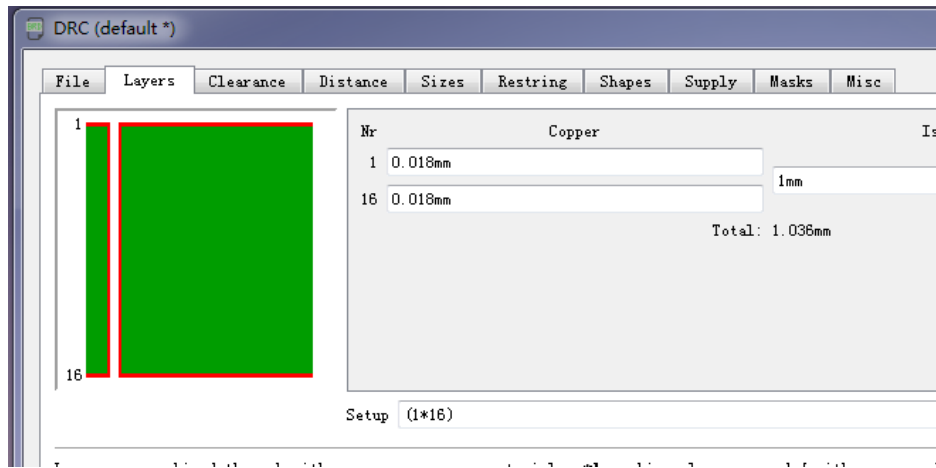
Fig.30 Project PCB layer setting

Some of the components need lay on the edge of the board in the project. The "Copper/Dimension" in the "DRC"->"Distance" panel should be set to 0mil.
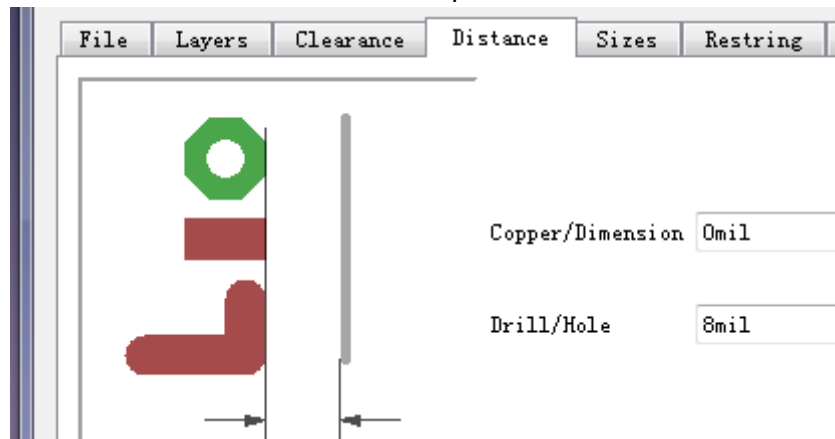
Fig.31 Distance setting

Other DRC rule can use the default value.

4.3 The final PCB design and production board

With the above steps and rules, the final design is shown following:

A. Power module
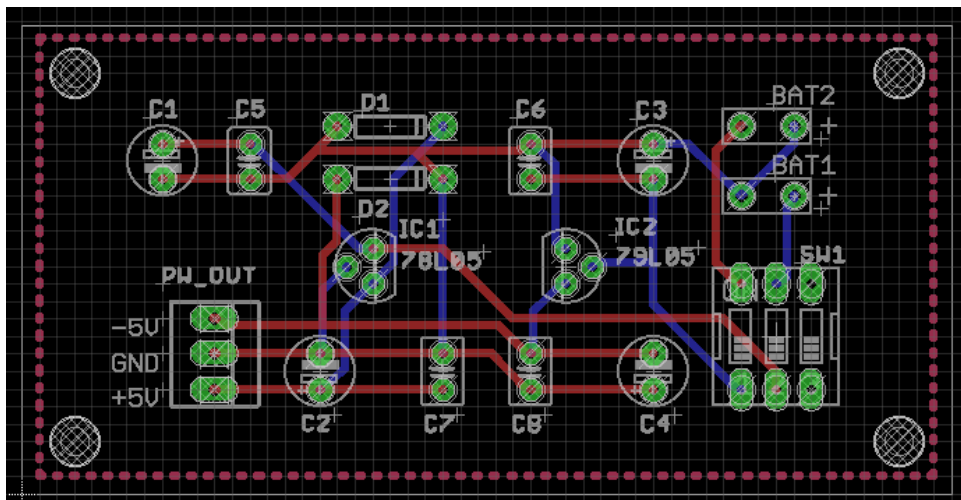
Fig.32 PCB of power module

B. DVM module

When install the components, the DVM and 2 buttons should be installed at back side of the board.
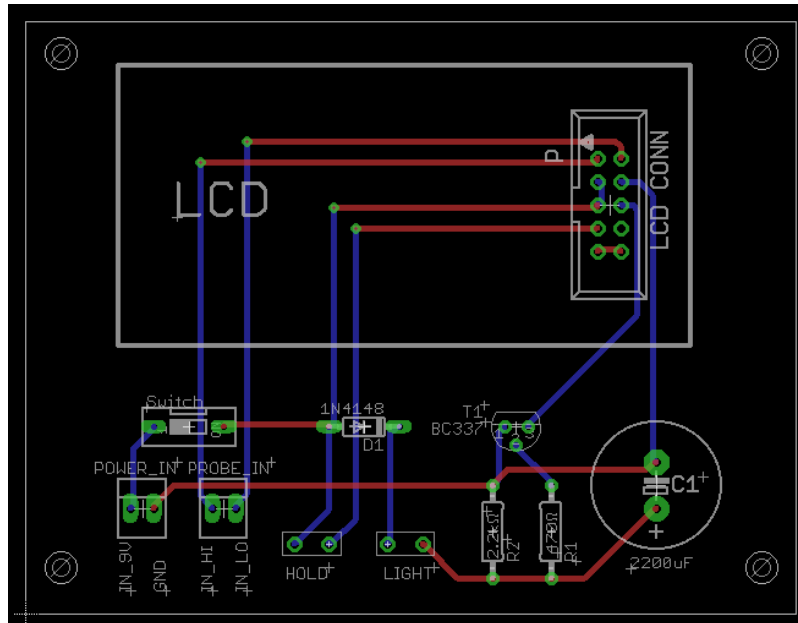
Fig.33 PCB of DVM module

C. Main board

The main board contains RF part (left small part) and DC analog part (right large part). The wide short line and a lot of via holes are used in RF part. Ground (copper-pour area) between two parts are connected with 0 Ohm resistor. In real board, several 0 Ohm resistors are used.
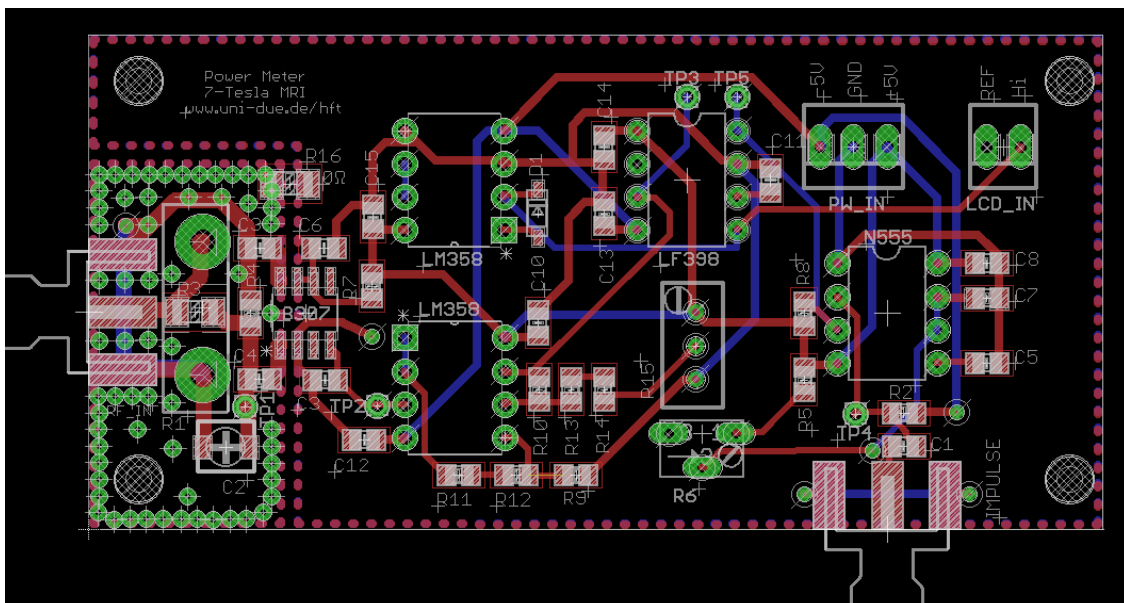
Fig.34 PCB line schematic
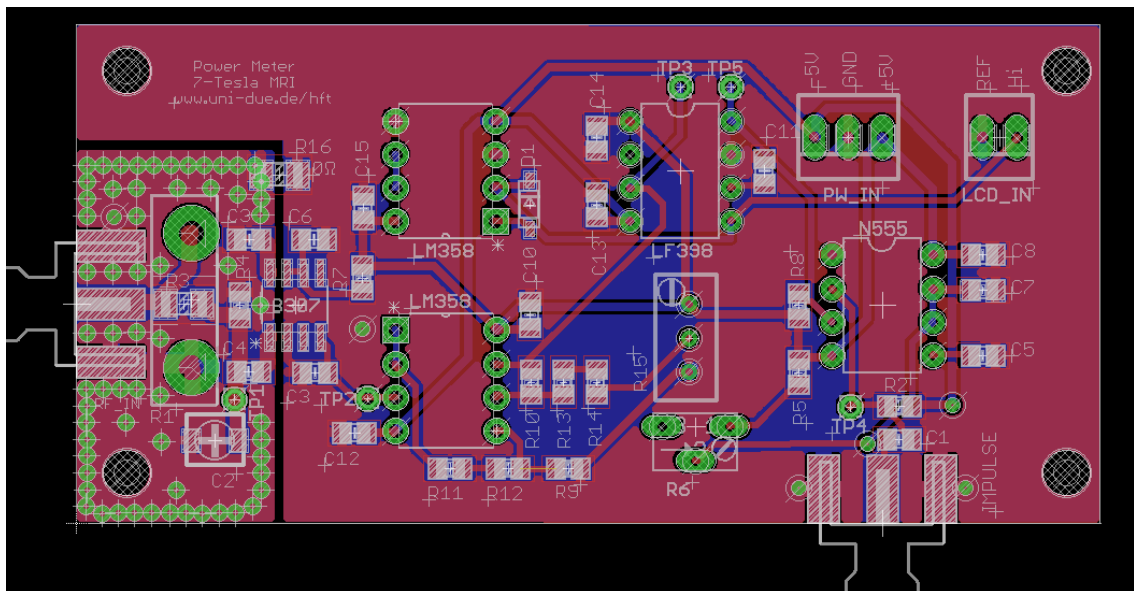
Fig 35 copper-pour ground in main module

D. The production board
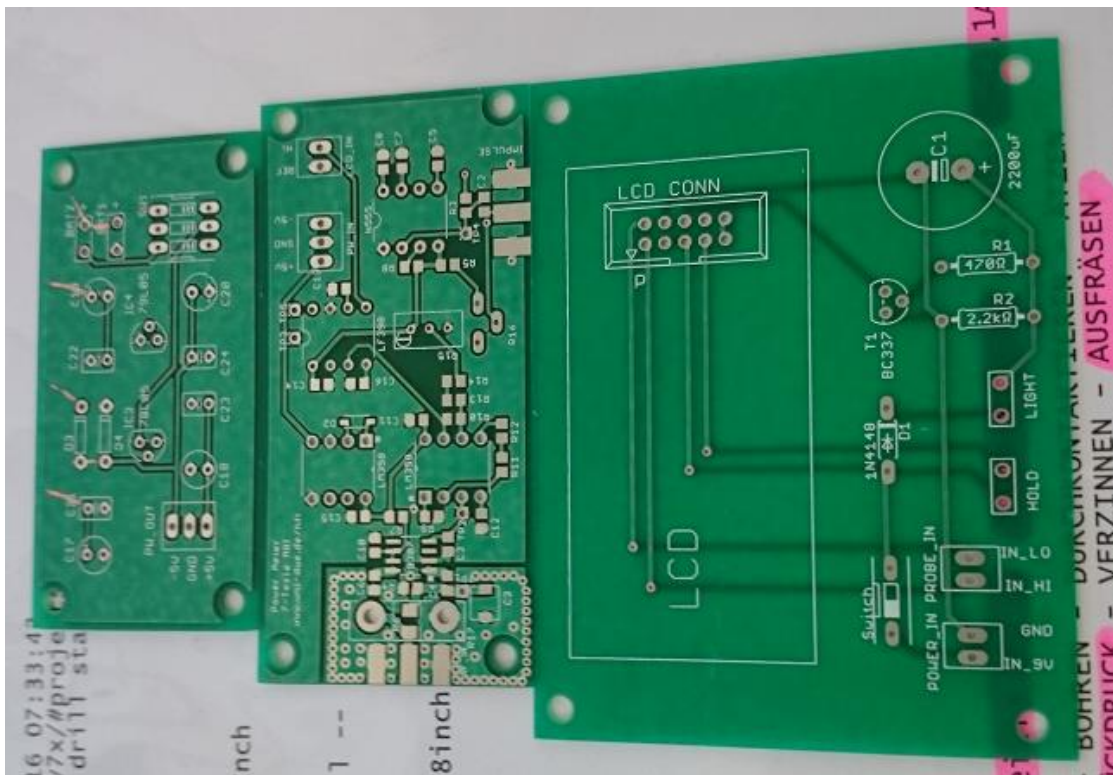
Fig.36 production board

5. System test

5.1 The introduction of test environment.

The main test devices are following:

- **Pulse signal generator**

Rigol DG1022 2 Channel 20MHz.

The pulse signal: 5Vpp with 95% duty cycle.

The inverse synchronous pulse signal will be feed to main board.

Fig.37 Pulse signal generator

- **RF signal generator**

Rohde & Schwarz 100kHz-2160MkHz

The RF signal 300MHz

Power output: -30dBm to 15dBm. The output power can be read directly on the panel.

Fig.38 RF signal generator

- **Oscilloscope**
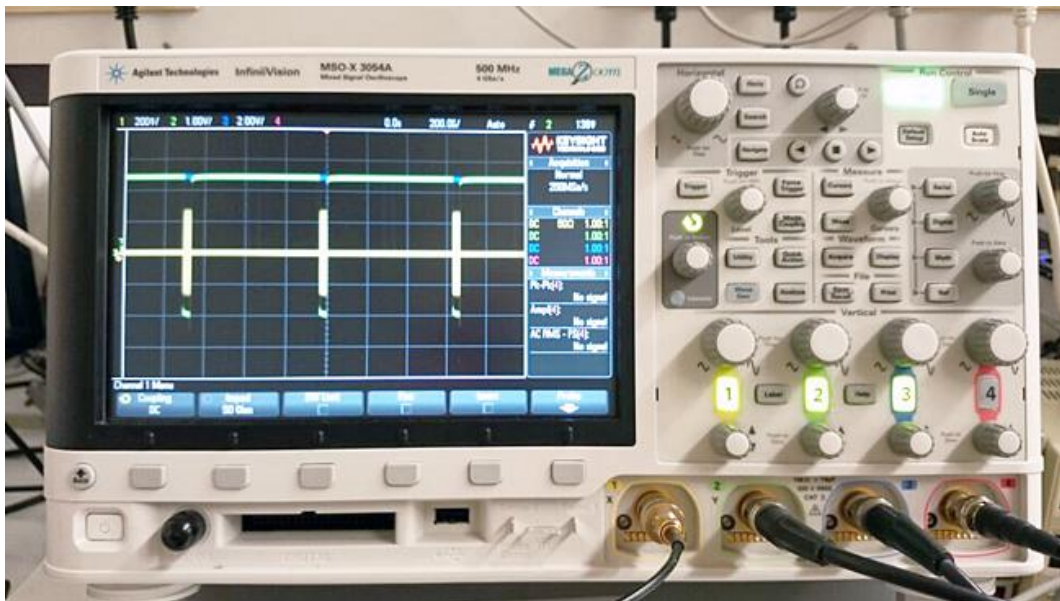
Fig.39 Agilent Oscilloscope

Agilnent MSOX3054A 500MHz

- **RF Amplifier**

Expand the test power rang to 40dBm

Fig.40 RF Amplifier

- **40dB attenuator**

Input protection for the oscilloscope.

- **The full system**

The 3 modules are assembled into a complete system
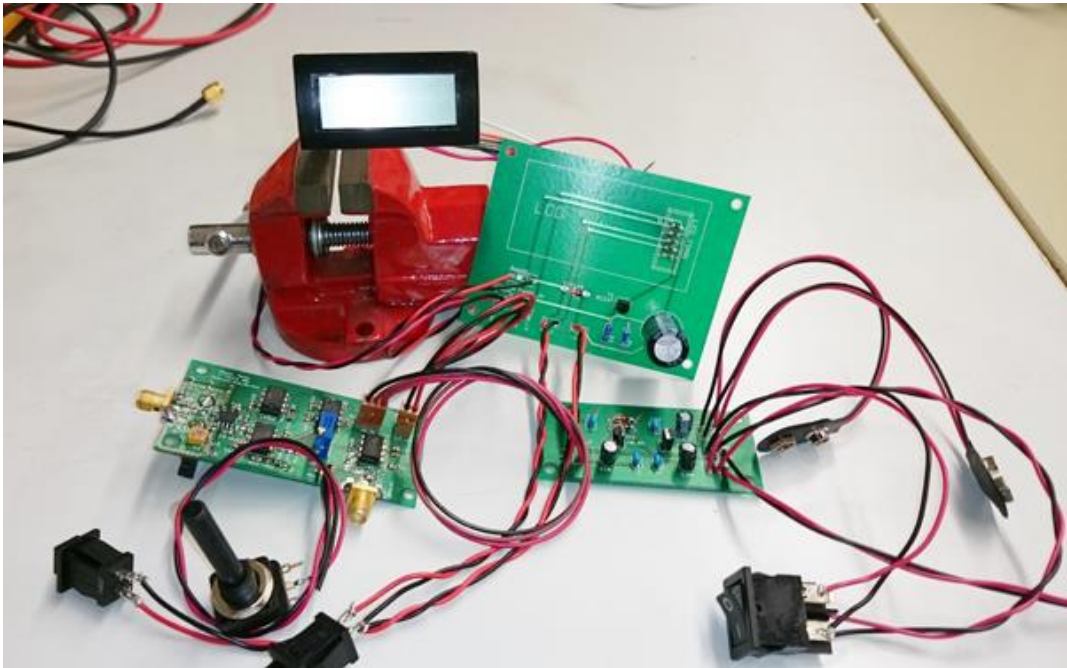
Fig.41 The full system

5.2 The Line loss (P_{loss}) measuring.
Connect the RF signal generator to the Oscilloscope.
Record the output power value on the RF generator panel and the voltage value shown on the oscilloscope.
Calculate the power value on the oscilloscope side.
Compare the difference of two power value get the line loss.
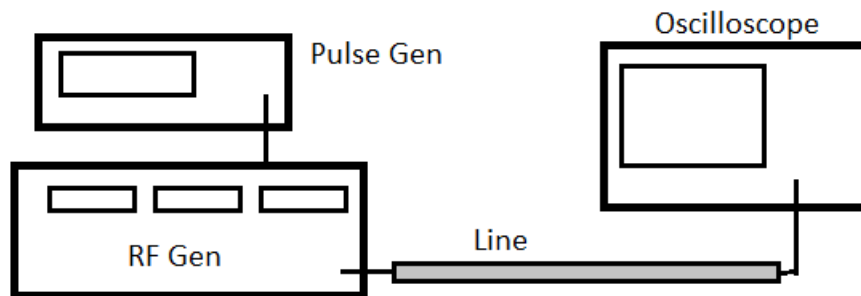
Fig.42 connection of line loss measuring

The table of measuring is shown as following:

Input from RF Gen (dBm)	Oscilloscope		line loss (dBm)
	Voltage (V)	Power (dBm)	
15.000	3.000	13.522	1.478
14.500	2.800	12.923	1.577

14.000	2.700	12.607	1.393
13.500	2.600	12.279	1.221
13.000	2.400	11.584	1.416
12.500	2.300	11.214	1.286
12.000	2.200	10.828	1.172
11.500	2.100	10.424	1.076
11.000	2.000	10.000	1.000
10.500	1.900	9.554	0.946
10.000	1.800	9.085	0.915
9.500	1.700	8.588	0.912
9.000	1.600	8.062	0.938
8.500	1.500	7.501	0.999
8.000	1.400	6.902	1.098
7.500	1.300	6.258	1.242
7.000	1.200	5.563	1.437
6.500	1.150	5.193	1.307
6.000	1.100	4.807	1.193
5.500	1.050	4.403	1.097
5.000	0.990	3.892	1.108
4.500	0.940	3.442	1.058
4.000	0.890	2.967	1.033
3.500	0.840	2.465	1.035
3.000	0.790	1.932	1.068
2.500	0.750	1.481	1.019
2.000	0.710	1.005	0.995
1.500	0.670	0.501	0.999
1.000	0.630	-0.034	1.034
0.500	0.600	-0.458	0.958
0.000	0.570	-0.903	0.903
Avg:			1.126

The voltage values read from oscilloscope are peak to peak value.
Thus the power calculation formula is following:

$$\text{Power in dbm} = 10 \cdot \log(\frac{(\hat{u})^2 \cdot 1000}{8R}), \text{ with R = 50}\Omega \qquad (14)$$

The line loss should be:

Line loss (difference) = Value of RF Generator − Value of Oscilloscope (15)

The measuring result of the line loss P_{loss} is about 1.1dBm.

5.3 The determination of the real ΔP.

The ΔP is the only uncertain value in the formula (6). In order to determine ΔP, the voltage value of TP1 and TP2 should be measured.
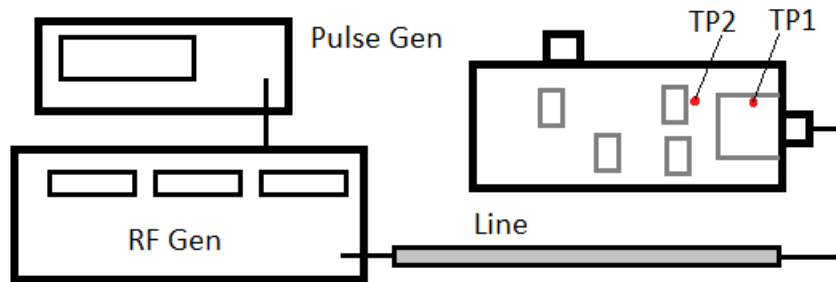
Fig.43 connection of ΔP measuring

With TP1, the output power P_m and ΔP can be calculated. Due to the measurement error, the ΔP is not a constant value.

Input dbm	Input with loss	TP1 / mV (AC rms)					Avg mV	P_m dBm	ΔP dBm
		1	2	3	4	5			
15	13.9	1.250	1.080	1.150	1.170	1.270	1.184	-45.523	-59.423
14	12.9	1.160	1.020	1.090	1.100	1.200	1.114	-46.052	-58.952
13	11.9	1.080	0.980	1.000	1.030	1.130	1.044	-46.616	-58.516
12	10.9	1.020	0.935	0.950	0.960	1.090	0.991	-47.068	-57.968
11	9.9	0.990	0.890	0.900	0.925	1.020	0.945	-47.481	-57.381
10	8.9	0.970	0.835	0.860	0.900	0.980	0.909	-47.818	-56.718
9	7.9	0.930	0.815	0.820	0.865	0.950	0.876	-48.140	-56.040
8	6.9	0.900	0.795	0.800	0.845	0.930	0.854	-48.361	-55.261
7	5.9	0.870	0.770	0.780	0.830	0.910	0.832	-48.587	-54.487
6	4.9	0.850	0.750	0.760	0.820	0.900	0.816	-48.756	-53.656
5	3.9	0.810	0.730	0.700	0.800	0.890	0.786	-49.081	-52.981

The voltage values read from oscilloscope are ac rms value.

Thus the power calculation formula is following:

$$\text{Power in dbm} = 10 \cdot \log(\frac{(U_{rms})^2}{1000R}), \text{ with R = 50Ω} \tag{16}$$

With TP2 and formula (3), a reference output power P_r can be calculated.

TP1 P_m dBm	ΔP dBm	TP2 V	P_r dBm
-45.523	-59.423	1.210	-39.6
-46.052	-58.952	1.190	-40.4
-46.616	-58.516	1.150	-42
-47.068	-57.968	1.130	-42.8
-47.481	-57.381	1.110	-43.6
-47.818	-56.718	1.090	-44.4
-48.140	-56.040	1.060	-45.6
-48.361	-55.261	1.030	-46.8
-48.587	-54.487	1.010	-47.6
-48.756	-53.656	0.980	-48.8
-49.081	-52.981	0.960	-49.6

Compare P_m and P_r, find the closest values of P_m and P_r. Then ΔP can be chosen. The selected ΔP is considered to be the constant attenuator coefficient.

The measuring result of the real ΔP is about 53.7dBm.

5.4 The determination of the initial voltage at TP3.
With the formula (6), the initial TP3 can be determined.

TP2 = 0.2V (when no input, output TP2 is about 0.2V.)
U_0 = 0.2V, P_0 = -80dBm (From data sheet)
ΔP = 53.7dBm

$$TP3 = \frac{0.2V - 0.2V + 0.025\frac{v}{dBm} \cdot (-80dBm) + 0.025\frac{v}{dBm} \cdot 53.7dBm}{0.025\frac{v}{dBm}}$$

$$= -26.3dBm \tag{17}$$

This initial TP3 value can be used as a calibration base value.
On the board, the real TP3 is measured in voltage. When calibrate the system, the TP3 should be -0.0263V.

5.5 The testing of rang from 0dBm to 15dBm.
After the setting of the initial TP3 value, the system can be test.

Directly connect the RF generator to the board with feeding the pulse signal to control the sampling. Record and compare the input and output power.
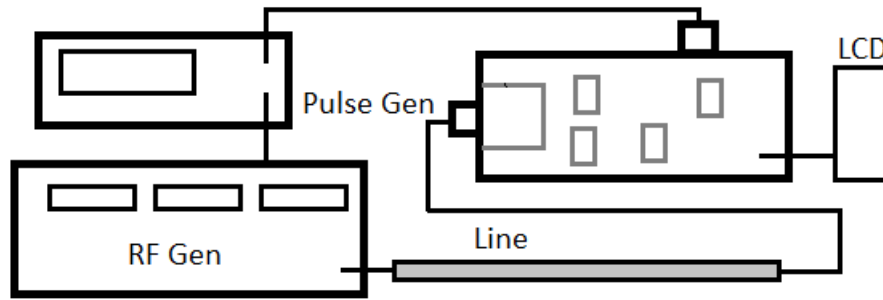
Fig.44 connection of testing of 0dBm to 15dBm

The measuring data list as follow:

RF input dBm	RF input after Line dBm	Power show on LCD dBm	Difference dBm
15	13.9	13.9	0
14	12.9	12.9	0
13	11.9	11.9	0
12	10.9	10.9	0
11	9.9	9.8	-0.1
10	8.9	8.9	0
9	7.9	7.8	-0.1
8	6.9	6.8	-0.1
7	5.9	5.8	-0.1
6	4.9	4.8	-0.1
5	3.9	3.8	-0.1
4	2.9	2.9	0
3	1.9	1.9	0
2	0.9	1	0.1
1	-0.1	-0.4	-0.3
0	-1.1	-0.4	0.7

The output example show as follow:

Fig.45 some results example

5.6 The testing of 12dBm to 42dBm with RF power amplifier.

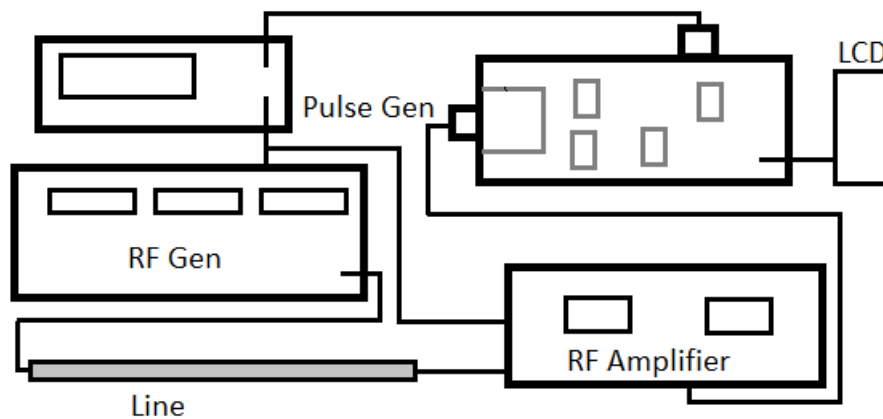Connect to the RF amplifier, the power rang 12dBm to 42dBm can be test.

Fig.46 connection of testing of 12dBm to 42dBm

The measuring data list as follow:

RF input dBm	Output with 40dB attenuator AC rms mV	Output Power +40dB dBm	Power show on LCD dBm	Difference dBm
3	257.50	41.23	41.80	0.57
2	255.50	41.16	42.10	0.94
1	249.70	40.96	42.00	1.04
0	241.20	40.66	42.20	1.54
-1	228.40	40.18	41.80	1.62
-2	210.90	39.49	40.90	1.41
-3	190.30	38.60	40.10	1.50
-4	170.90	37.67	38.80	1.13
-5	151.50	36.62	37.60	0.98
-6	134.50	35.58	36.40	0.82
-7	126.00	35.02	35.60	0.58
-8	106.50	33.56	33.80	0.24
-9	93.50	32.43	32.80	0.37
-10	83.80	31.48	31.70	0.22
-11	74.50	30.45	30.60	0.15
-12	66.00	29.40	29.70	0.30
-13	59.30	28.47	28.70	0.23
-14	51.90	27.31	27.80	0.49
-15	47.80	26.60	26.90	0.30
-16	42.90	25.66	25.90	0.24
-17	38.30	24.67	25.00	0.33
-18	34.70	23.82	23.90	0.08
-19	30.80	22.78	23.00	0.22
-20	27.80	21.89	22.00	0.11
-21	24.90	20.93	21.00	0.07
-22	22.30	19.98	20.00	0.02
-23	19.80	18.94	19.00	0.06
-24	17.80	18.02	18.20	0.18
-25	16.10	17.15	17.20	0.05
-26	14.30	16.12	16.30	0.18
-27	12.60	15.02	15.40	0.38
-28	11.20	13.99	14.40	0.41
-29	9.90	12.92	13.50	0.58
-30	9.00	12.10	12.40	0.30

The output example show as follow:

Fig.47 some results example

6. Conclusion and Discussion

After test, the system can operate under the expected conditions and give a relatively accurate, linear measuring results in rang 0dBm to 40dBm.

Some points in system may need to discuss or improve.
1. System outputs 0 dBm, when there is no input.
The DVM module cannot show other symbol or characters to represent a meaning "no output". The 0 dBm is small enough to be a start point of the measure range.

2. In the 12dBm to 42dBm, the max measure error in the high power.
The problem may be caused by the RF amplifier. The power restrict in peak of wave form and the result is not linear.

3. The full 1kW input is not test because limitation of the laboratory conditions. May could be some new problem in full power test.

Reference

About HF behaviors of passive component

1. Script: Microwave and RF Technology by Prof. DR.-Ing. K. Solbach.
   Page 32-49 Passive Linear circuit elements

2. Equivalent Circuit Description for SMD-Components by Owais Imam Supervised by Prof. Dr.-Ing. Klaus Solbach
   From: http://hft.uni-duisburg-essen.de/arbeiten/

3. Handbook of Microwave Component Measurements: with Advanced VNA Techniques
   By Joel P. Dunsmore.   Page 33-35, SMT Resistor

About RC and 555 applications

4. Analog and Digital Electronics by U.A.Bakshi, A.P.Godse chapter4. All about 555 timer.

5. Circuits and Networks by U.A.Bakshi, A.V.Bakshi.   Page24-37 RC circuit.

6. http://pcbheaven.com/circuitpages/LED_Off_Delay

About power supply design

7. Electronics Devices And Linear Circuits by U.A.Bakshi, A.P.Godse chapter10   Voltage regulator

8. Linear Integrated Circuits by Salivahanan p364 IC voltage regulator

About EAGLE PCB design

9. Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards by Simon Monk

10. Printed Circuit Board Designer's Reference: Basics by Christopher T. Robertson