UNIVERSITÄT DUISBURG ESSEN

# Fachgebiet Hochfrequenztechnik

H F T

Fachbereich Ingenieurwissenschaften
Abteilung Elektrotechnik und Informationstechnik
Institut für Nachrichten- und Kommunikationstechnik

Prof. Dr.-Ing. K. Solbach
Prof. Dr.-Ing. A. Beyer

## Studienarbeit / Bachelorarbeit

### Aufgabe der Abschlussarbeit im ISE Bachelor/Masterstudiengang

**für:** Herrn Adam Rydygier

**gestellt von:** Prof. Dr.-Ing. K. Solbach
Fakultät für Ingenieurwissenschaften - Hochfrequenztechnik

**Aufgabestellung:** **3D simulation of high-speed serial interface design**

The multimedia world is continuously moving towards services that show enhanced performance and quality. Key challenge in the design of multimedia devices is interconnect. This topic is handled intensively in working groups like the Mobile Industry Processor Interface (MIPI) Alliance that is a consortium of around 100 worldwide operating companies. High-speed serial interfaces are alternatives to traditional parallel interfaces, as they save pins and area. However, design of high-speed chip-to-chip interfaces is challenging due to the occuring high frequencies. Parasitic effects of chip package and printed circuit board may significantly reduce the performance of the interface.

This thesis covers investigations on an existing physical layer IC implementation on a testchip in 65 nm CMOS technology. The testchip contains a pre-version for the D-PHY standard defined by MIPI. It consists of the physical layer, including drivers and receive circuitry. In this thesis a 3D model of the parasitic effects due to chip assembly is developed by using the 3D simulation tool “Microwave Studio” from CST. The model has to consider the chip package, including bond wires, package leads and pins, and PWB wires. The resulting model should be suitable for being included in the Spice-based electrical simulation of the transmitter and receiver circuits.

Target of this work is to understand the impact of the package and board related parasitic effects on the existing implementation. The simulation should focus on coupling effects, especially from data lines to power supply. The model should give information about induced ripples on the supply voltage directly at the electrical device. Measurements can not access this circuit node since it is inside the package; it is just possible to measure at the package pin. From the results instructions for required power supply decoupling capacitors (on-chip and on-board) should be worked out.

*Work breakdown*

Part 1:

- Study of high-speed serial interfaces
- Study of 3D simulation basics and usage of Microwave Studio
- Understand the implemented circuit and its application
- Input of the interface structure (package, bond wires, etc.) to 3D-simulator Microwave Studio
- 3D simulation, resulting in Spice model

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Part 2:

- Set up a Spice level test bench for investigation of signal coupling to supply lines
- Include the 3D Spice model into the testbench
- Runnig Spice level simulations that include 3D parasitic effects
- Propose circuit design for improvement

Part 3:

- Documentation
- Presentation of results

At the end of the thesis work, a public presentation is to be given of the results.