Driver Amplifier for 7–Tesla MRI Smart Power Amplifier

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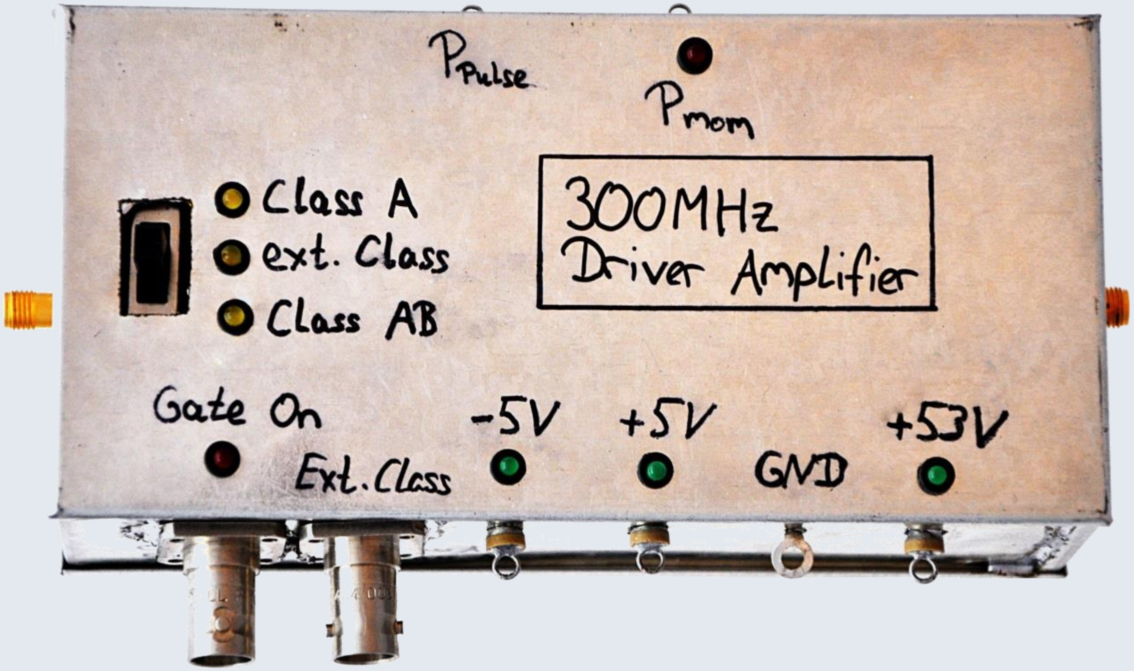
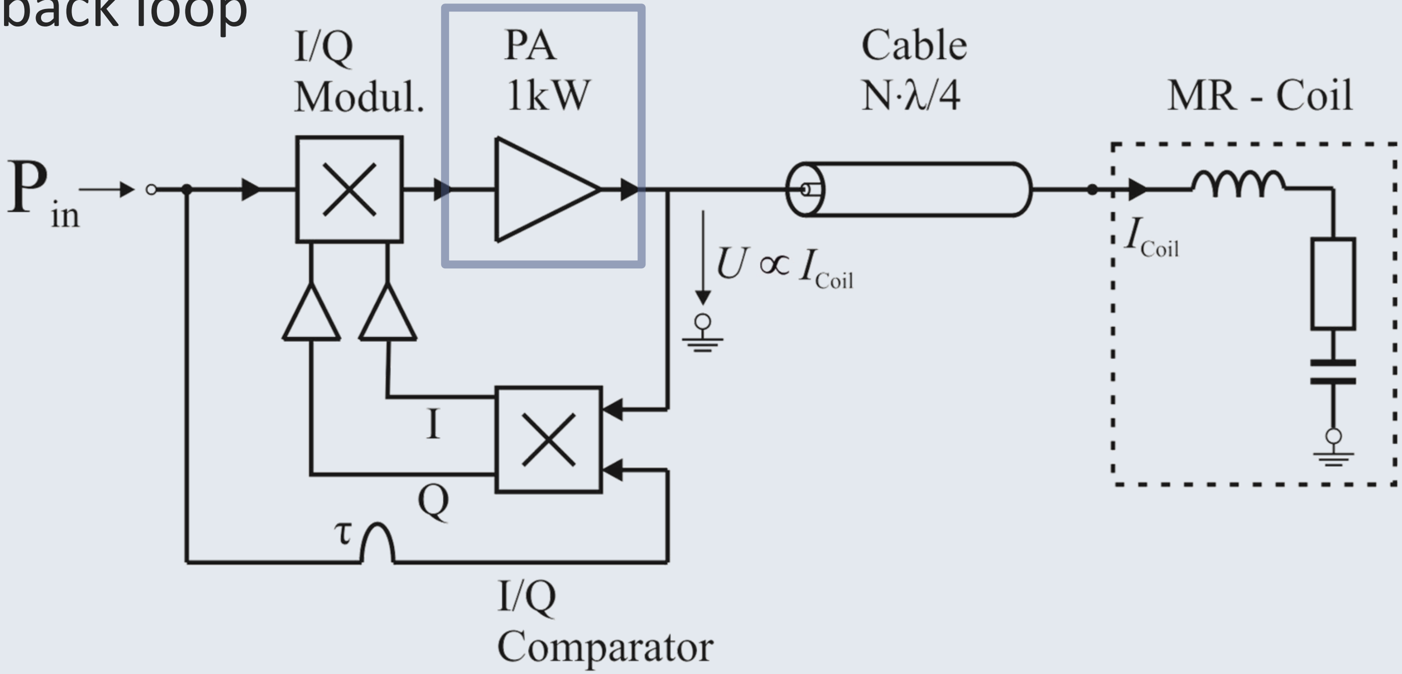
Contents

- Introduction
- Concept
- Power Amplifier
- Gate Bias Circuit
- Voltage Regulator
- Power Monitor
- Assembly
- Conclusion



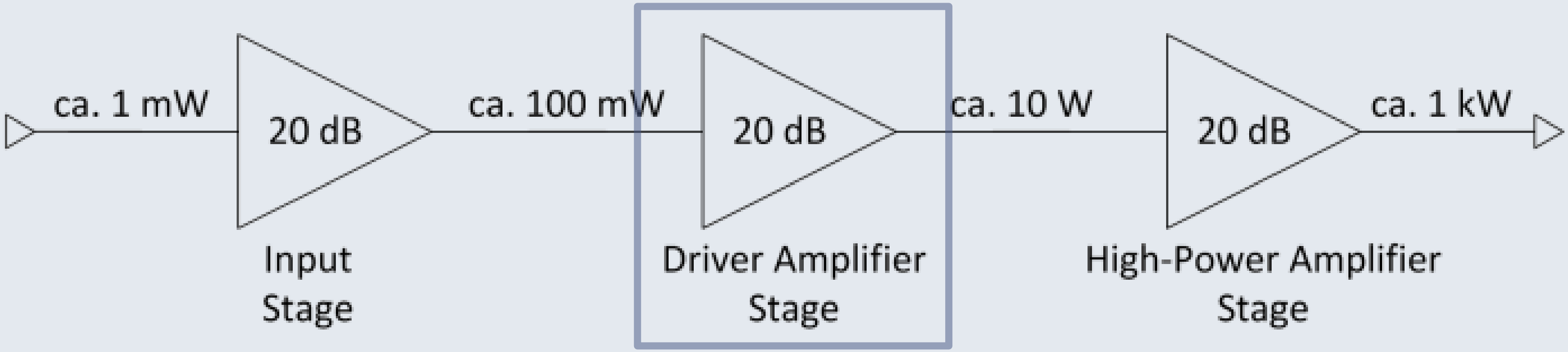
Introduction

- 7 – Tesla MRI system employs 32 channels, each of which can produce 1 kW of pulsed power at 300 MHz
- each channel consists of an RF power amplifier and a cartesian feedback loop



Introduction

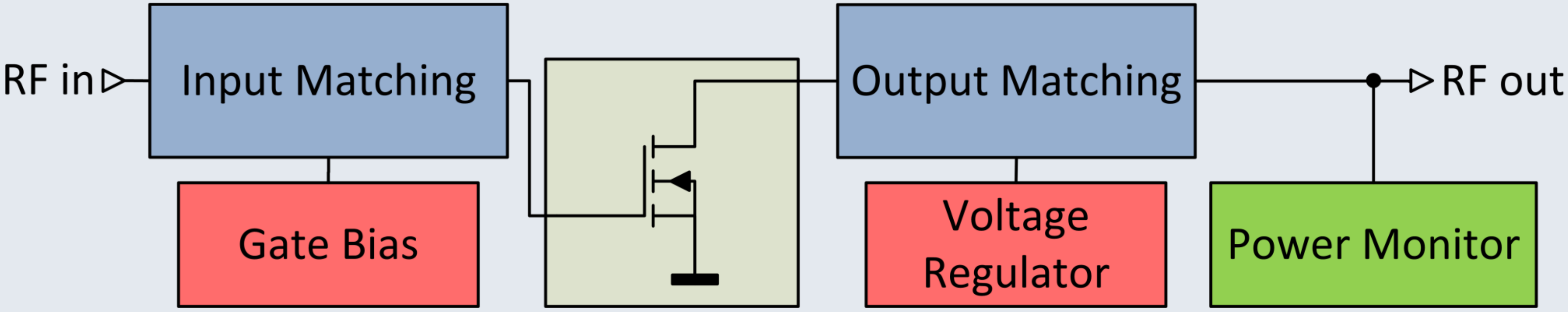
- 1 kW – power amplifier:



- Driver Amplifier will be used to evaluate some concepts for the driver and high-power stage, e.g.
  - Temperature Compensation
  - Power Monitor

Concept

- Driver Amplifier can be divided into five sub – circuits:



- Operating Point Stabilization
- Class A / Class AB Switching
- Temperature Compensation
- On / Off Switching

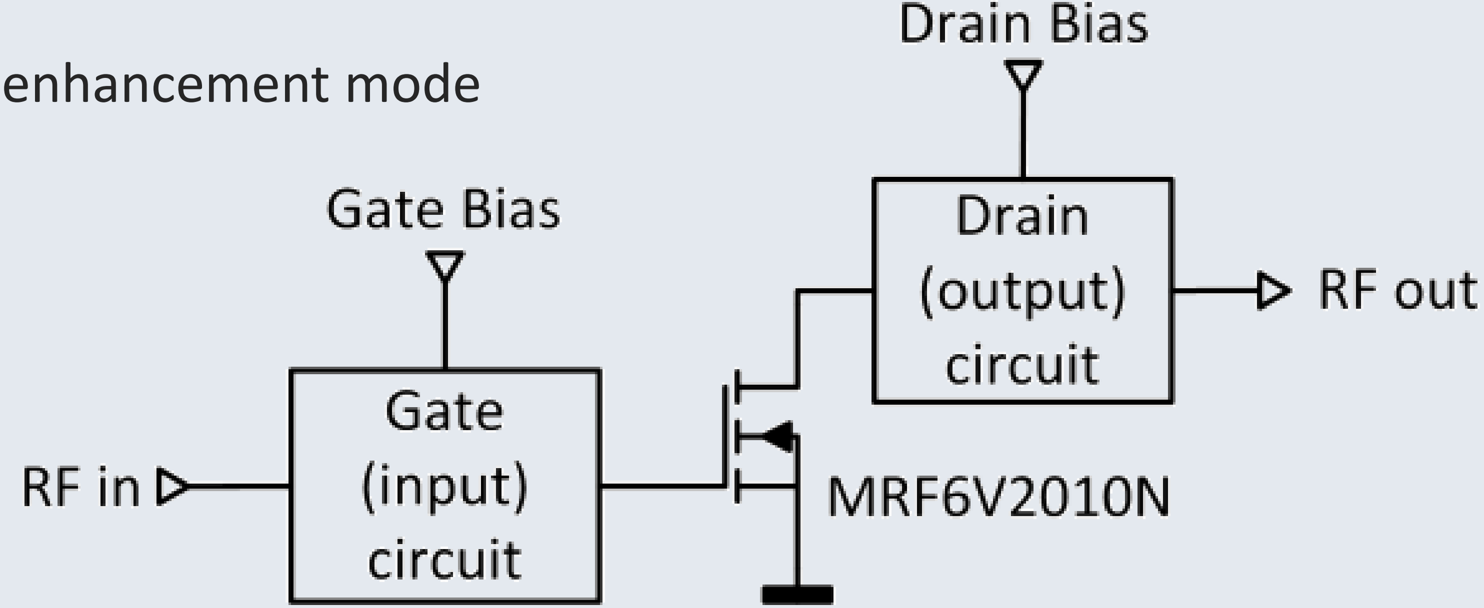
- Drain – Source Voltage Stabilization
- Load Regulation

- Easy & precise monitoring of
  - pulse power
  - momentary power

Power Amplifier

Power Amplifier Concept

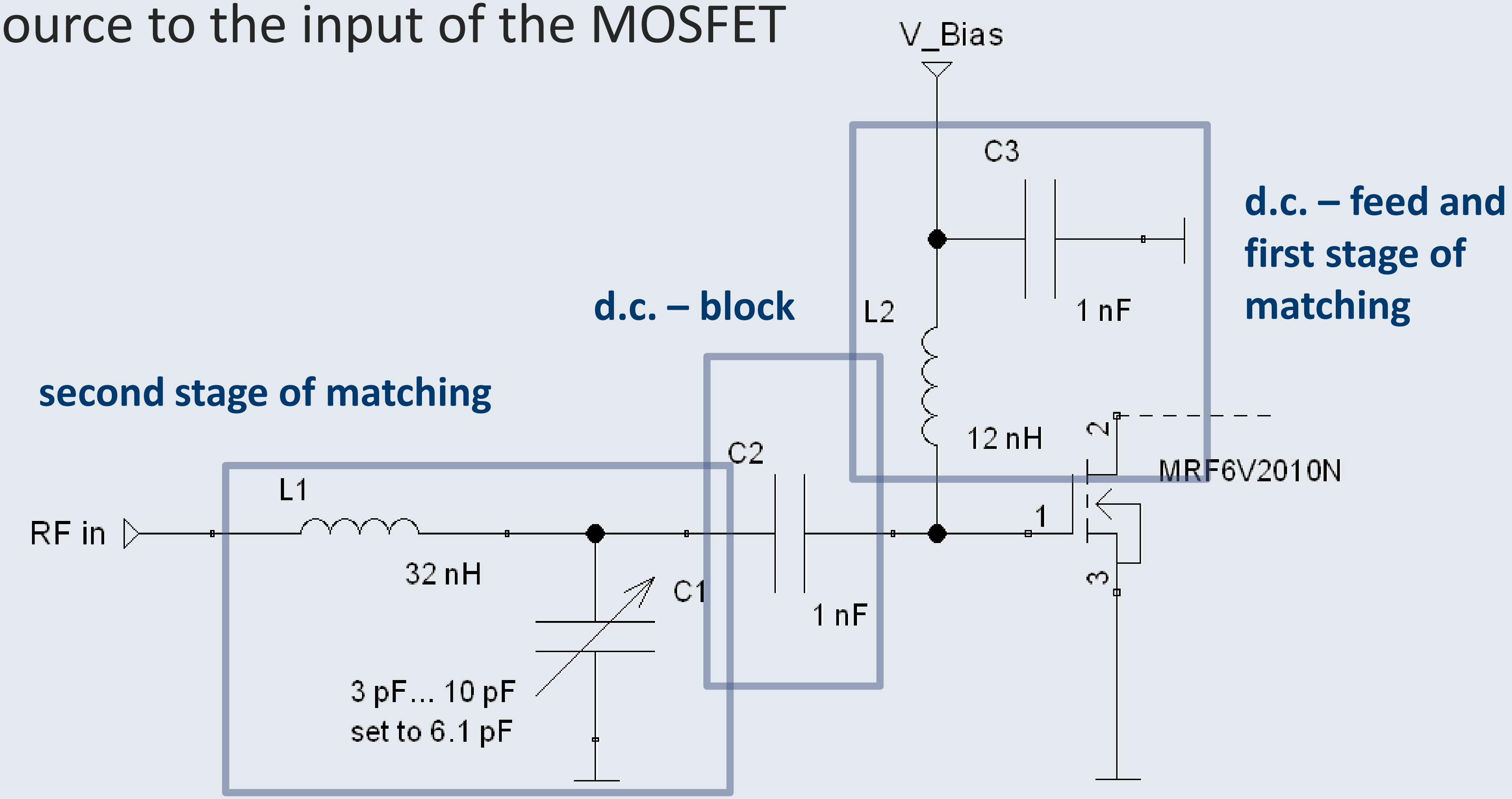
- Power amplifier is built around a Freescale MRF6V2010N
  - RF power MOSFET
  - n – channel
  - enhancement mode



Power Amplifier

Input Circuit

- Input circuit provides d.c. – feed and matching of the 50 Ω – source to the input of the MOSFET



d.c. – feed and first stage of matching

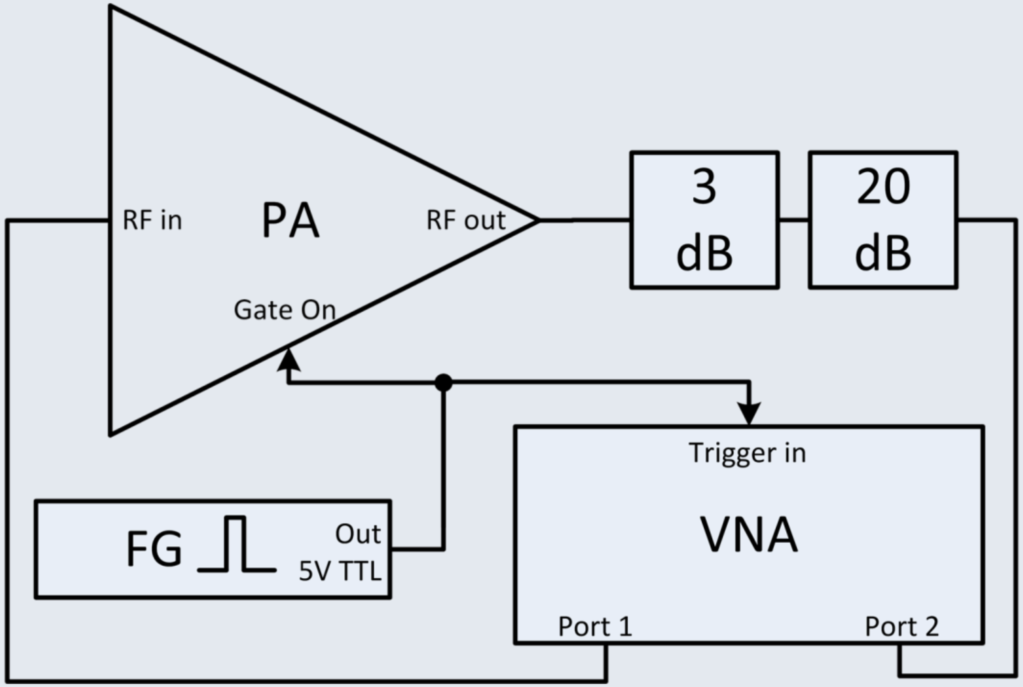
d.c. – block

second stage of matching

Power Amplifier

Input Reflection Coefficient S_{11}

- Best match has been achieved with the two–stage matching network, that is however quite different from the manufacturer's recommendation
- Input reflection coefficient S_{11} has been measured with a vector network analyzer (VNA) for a Class A and a Class AB operating point



Power Amplifier

Input Reflection Coefficient S_{11}

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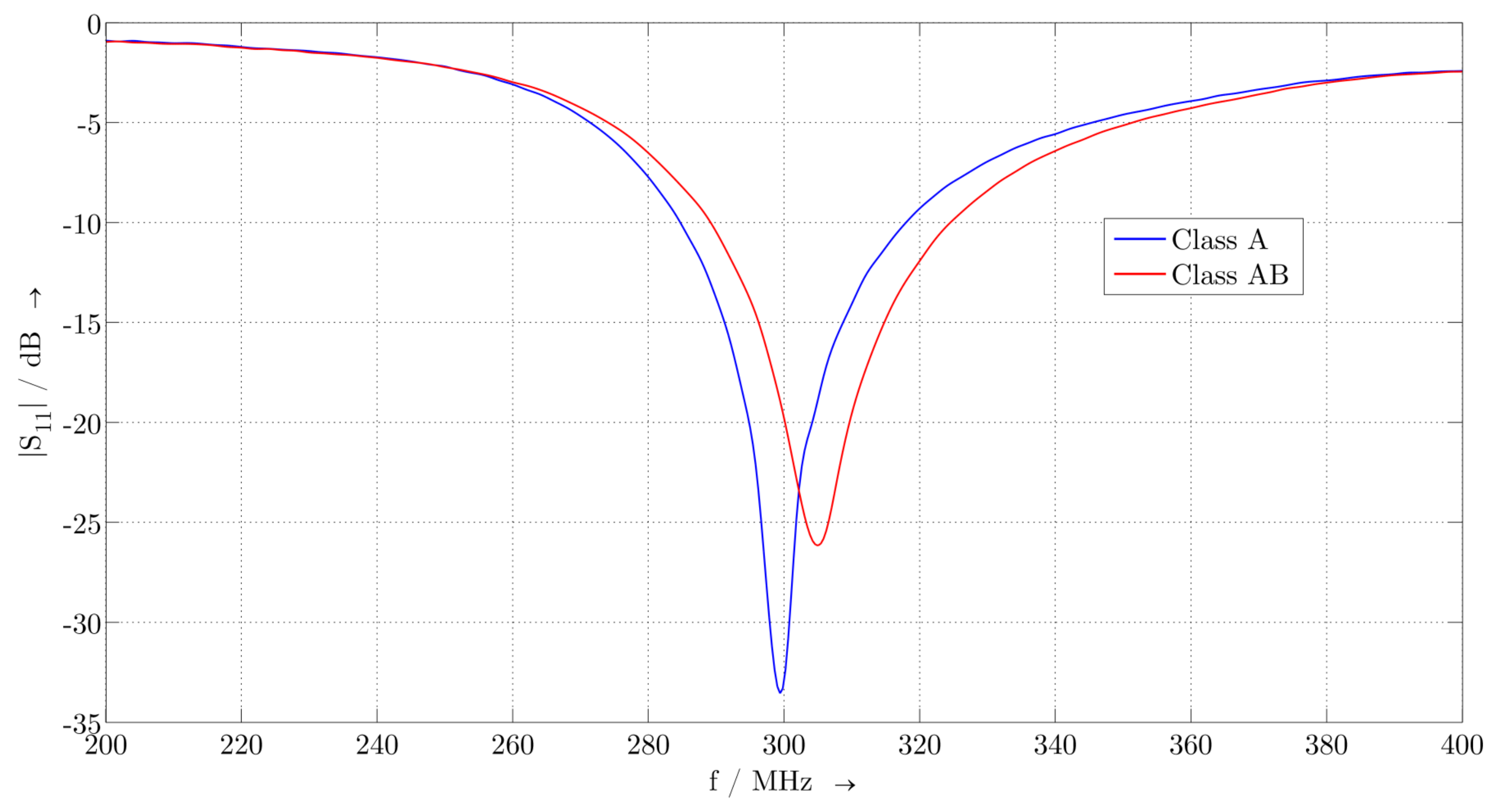
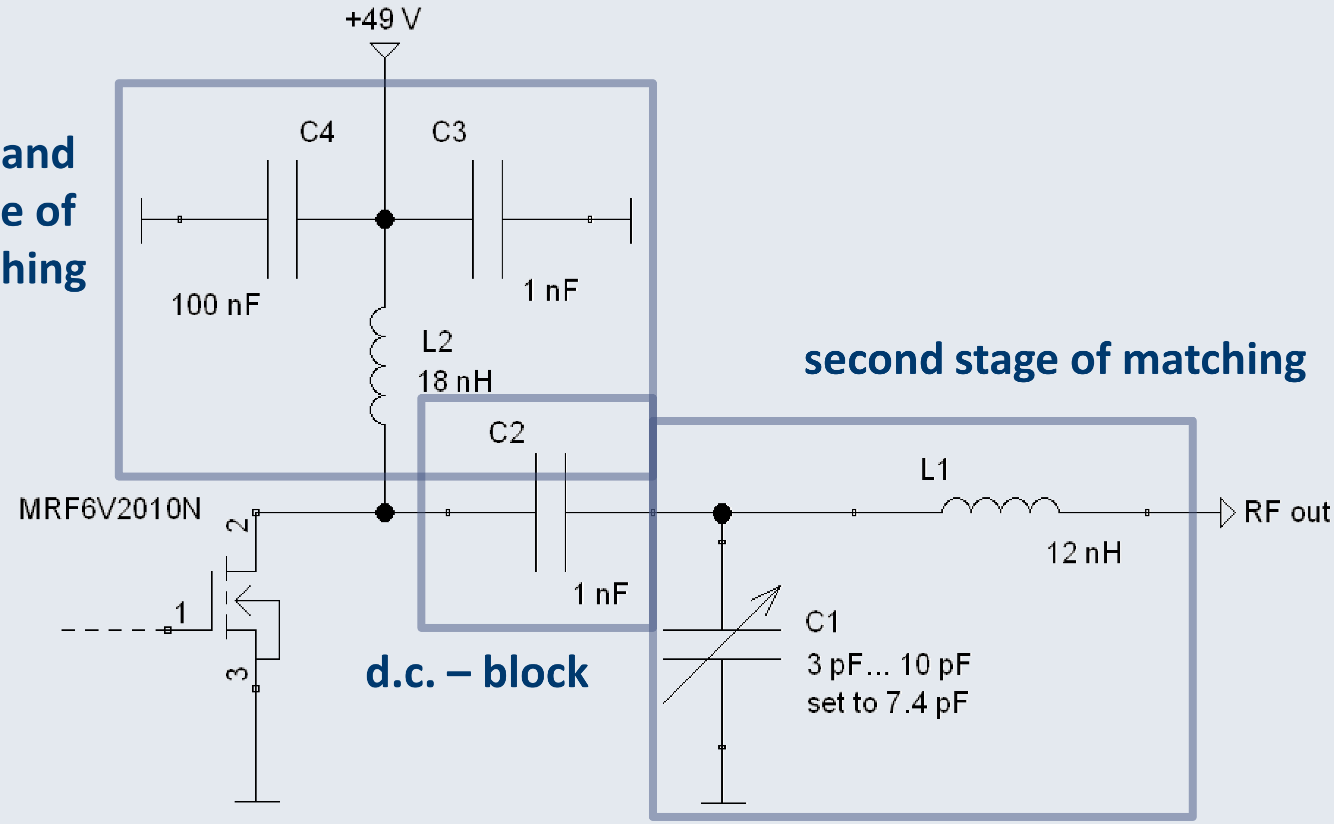
- Small signal (P_{in} = 0 dBm) input reflection coefficient S_{11} as measured with VNA



Power Amplifier

Output Circuit

- Output circuit provides d.c. – feed and matching of the output of the MOSFET to the 50 Ω – load



d.c. – feed and first stage of matching

second stage of matching

d.c. – block

Power Amplifier

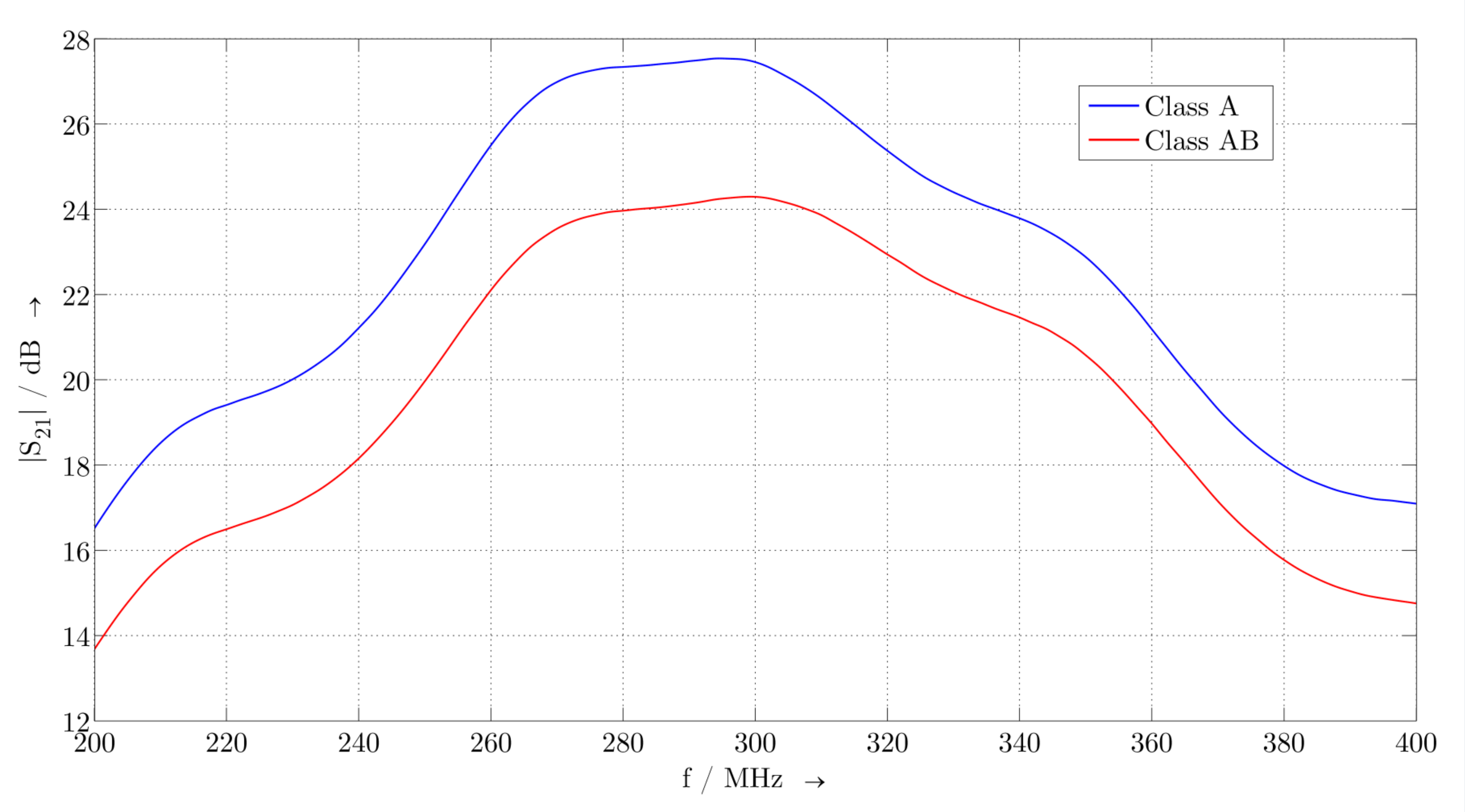
Power Gain

- Power gain (forward transmission coefficient S_{21}) is determined by
  - operating point
  - input power
  - quality of the input and output matching networks
- Power gain has been measured with
  - vector network analyzer (VNA)
  - RF signal generator and power meter
  - (RF signal generator and spectrum analyzer)

Power Amplifier

Power Gain

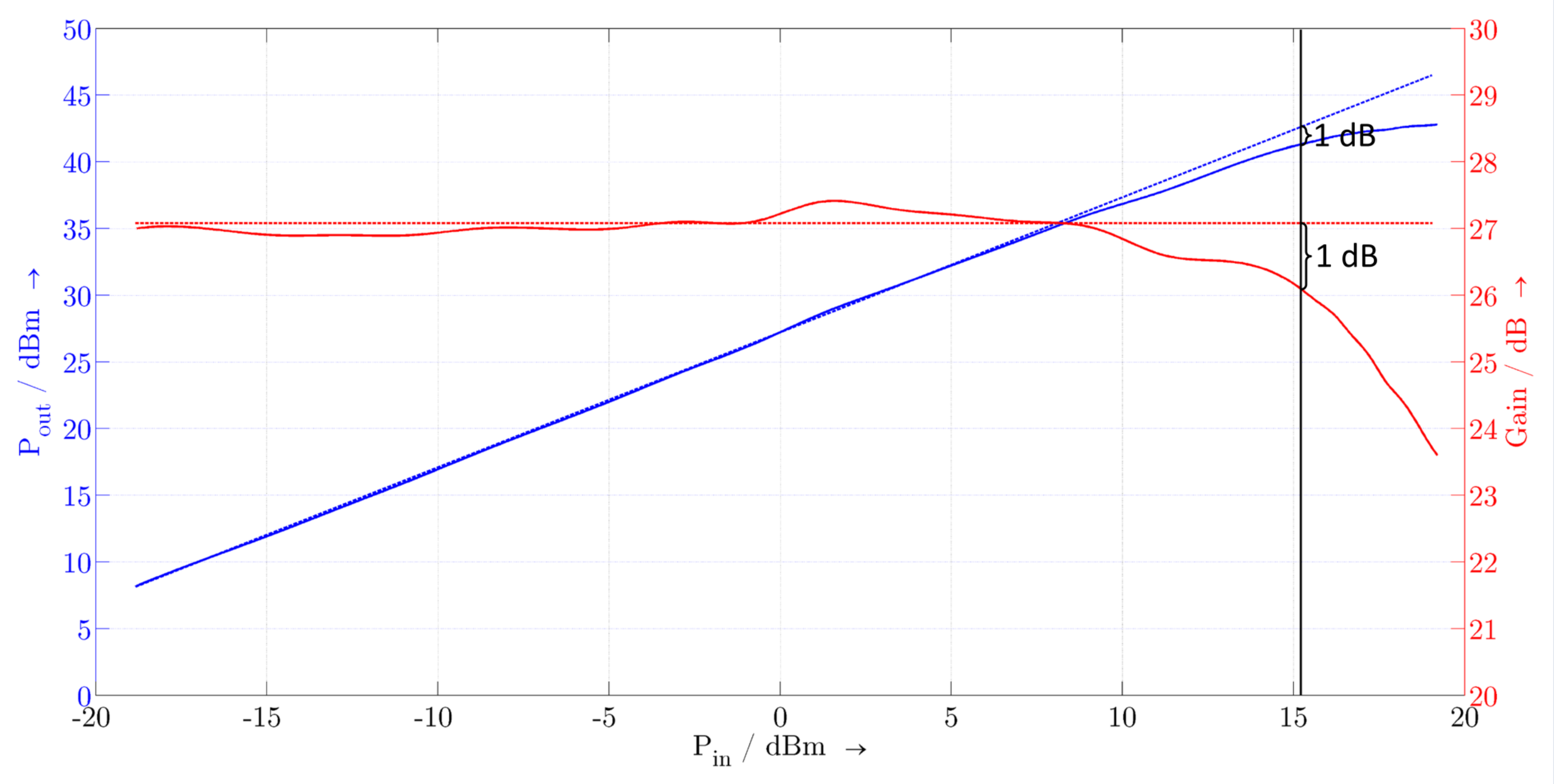
- Small signal (P_{in} = 0 dBm) power gain S_{21} as measured with VNA



Power Amplifier

Power Gain

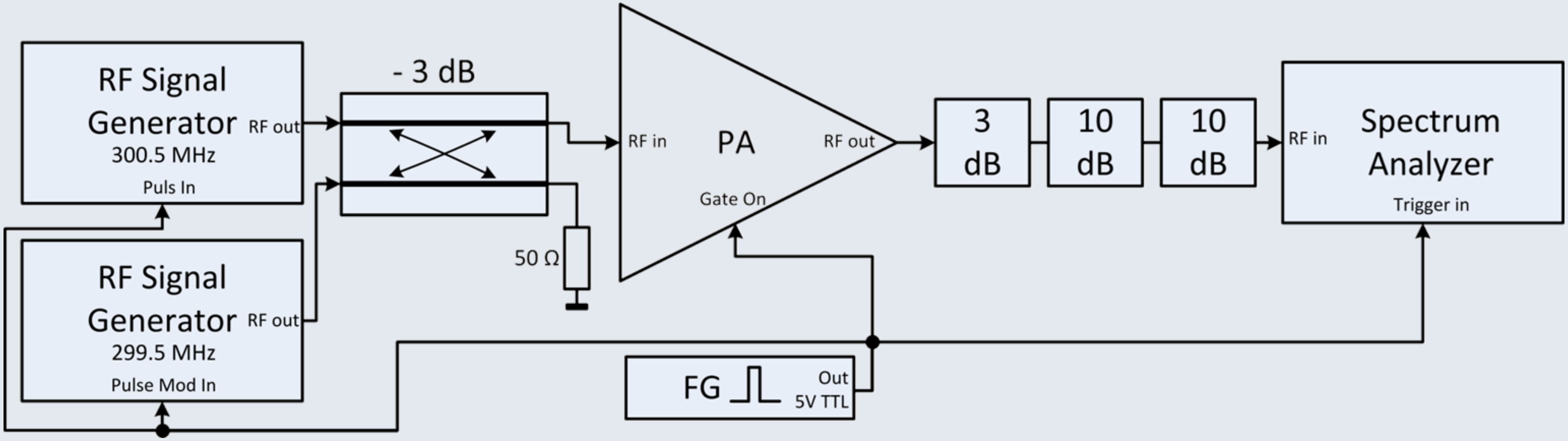
- Power gain and P_{1dB} as measured with RF signal generator and power meter



Power Amplifier

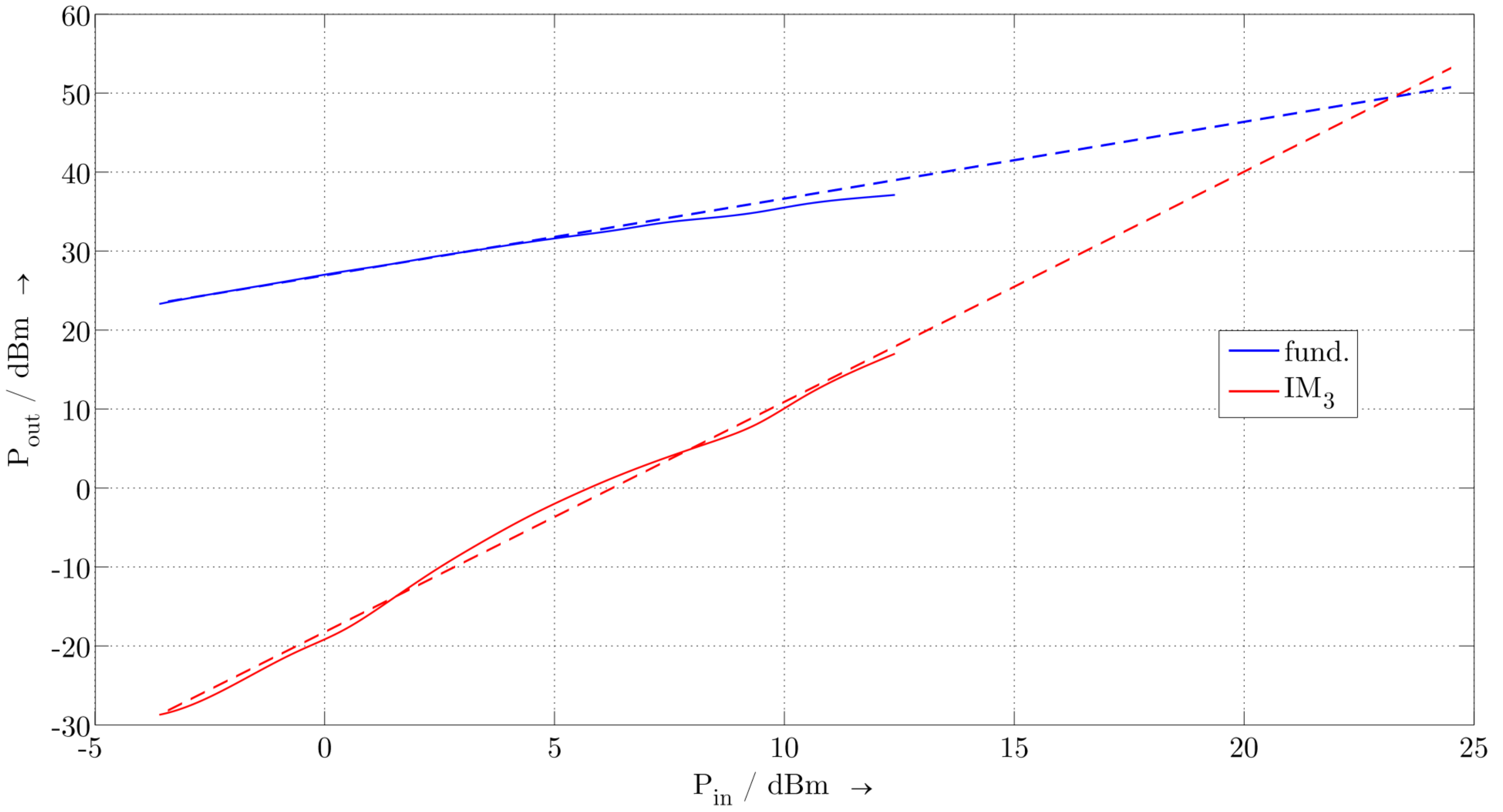
Intermodulation Distortion

- Third – order intermodulation products are not affected by output filter, so they can be used to quantify the harmonic distortion caused by the MOSFET.
- Third – order intercept point has been measured with a two – tone measurement:



Power Amplifier

Intermodulation Distortion



Power Amplifier

Summarized Data

	VNA	Power Meter	Spectrum Analyzer	Datasheet
Input Reflection Coefficient S_{11} (P_{in} = 1 mW / 0 dBm)	– 33 dB			
Small signal power gain (P_{in} = 1 mW / 0 dBm)	27.5 dB	27.1 dB		ca. 24 dB
$P_{1\text{dB}}$		15.2 dBm		ca. 17.3 dBm
Maximum Output Power (P_{in} = 100 mW / 20 dBm)		19.1 W / 42.8 dBm		12.6 W / 41 dBm
IIP_3			23.2 dBm	
OIP_3			49.5 dBm	

These values need some discussion!

Power Amplifier

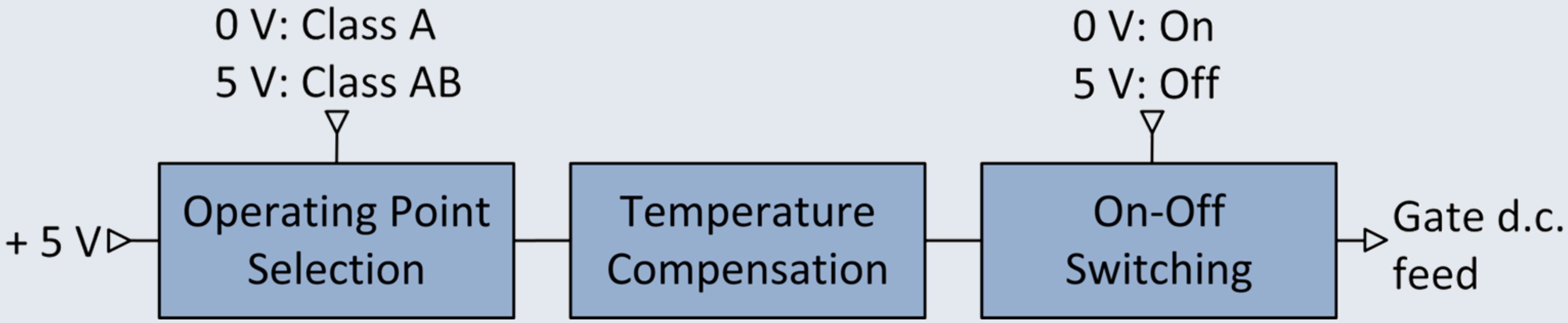
Discussion

- Small signal power gain and maximum output power strongly exceed the values to be expected from the datasheet.
- Explanations:
  - Measurements have been performed with three different principles, leading to similar results → plausible
  - Measurements at V_{GS} = 3.4 V (Class A); datasheet values at I_{DQ} = 30 mA (corresponding to $V_{GS} \approx$ 2.6 V; close to Class B)
  - Measured input return loss S_{11} is approx. –33 dB; datasheet values are between –14 and –9 dB
  - Input and output matching networks are quite different from the networks in the datasheet, both in architecture and component values

  → realized matching networks are supposedly better than the manufacturer‘s

Gate Bias Circuit

Concept



0 V: Class A
5 V: Class AB

0 V: On
5 V: Off

+ 5 V

Operating Point Selection

Temperature Compensation

On-Off Switching

Gate d.c. feed

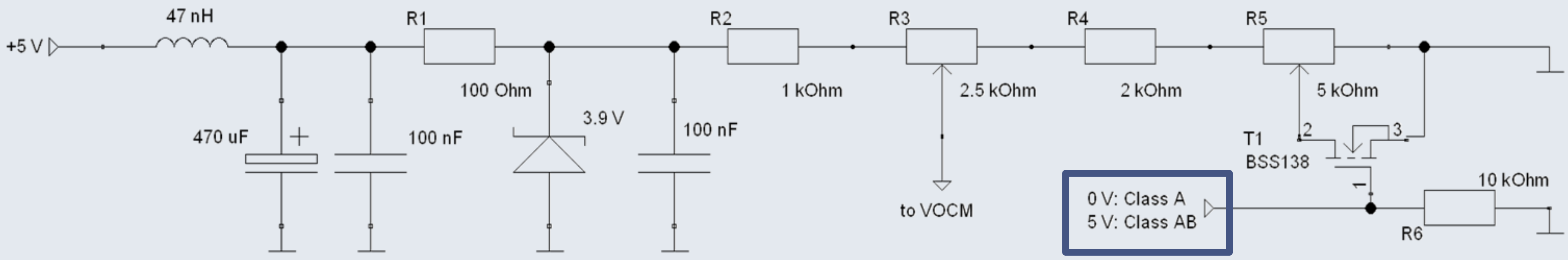
- Operating Point Stabilization
- Choosing a Class A and a Class AB operating point
- Switching between these two points

Temperature stabilization of the quiescent current

Fast switching between the designated gate bias voltage and $V_{GS} = 0$ V

Gate Bias Circuit

Operating Point Selection



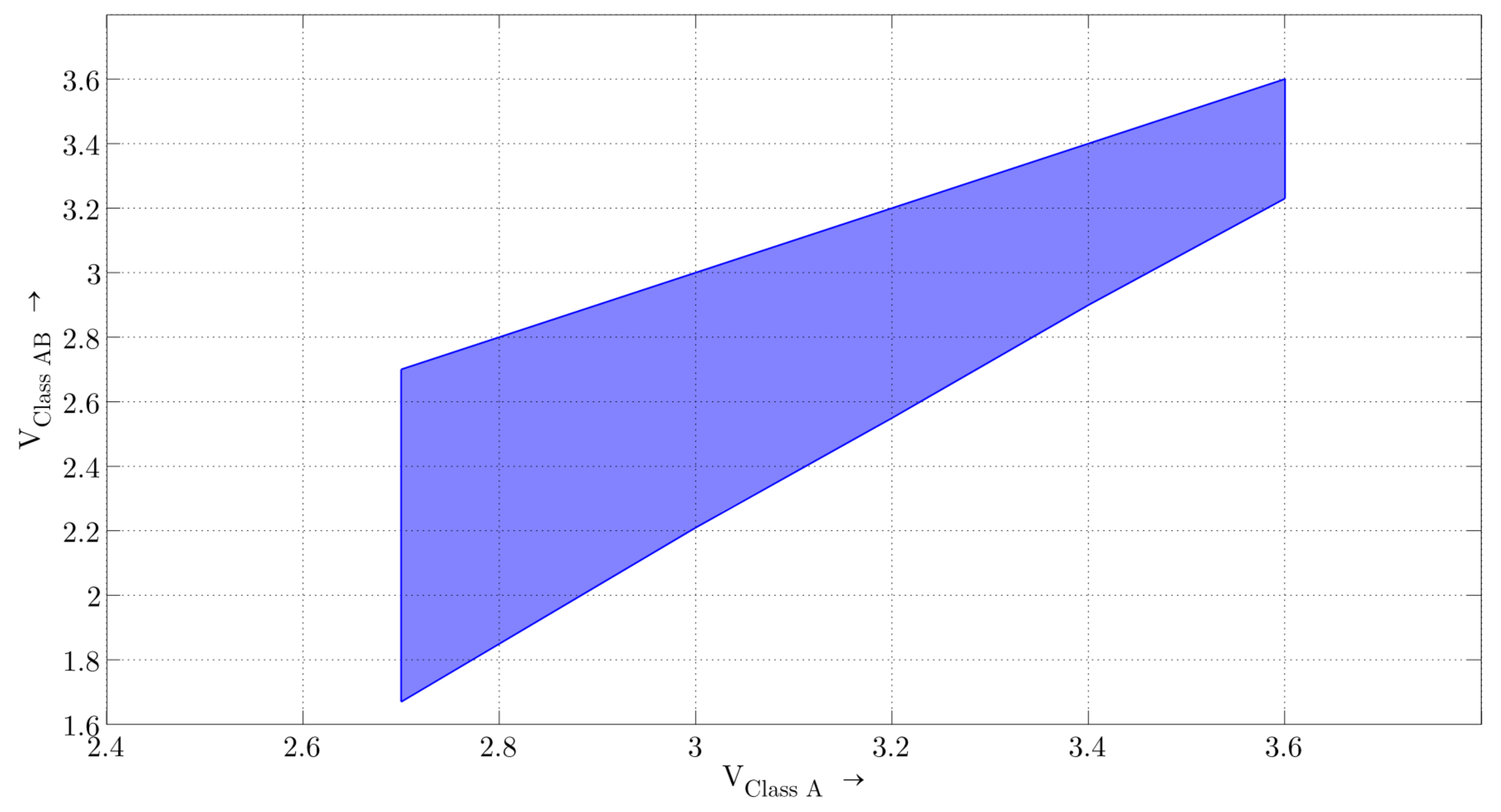
TTL input

- Input voltage is stabilized against ripple and noise on the power supply rail with low-pass filter and Zener diode.
- One potentiometer (R_3) allows the selection of the Class A operating point.
- A portion of a second potentiometer (R_5) is bypassed by a logic-level MOSFET T1 when a voltage of 5 V is applied at its gate.
- This potentiometer determines the distance between the Class A and the Class AB operating point.

Gate Bias Circuit

Operating Point Selection

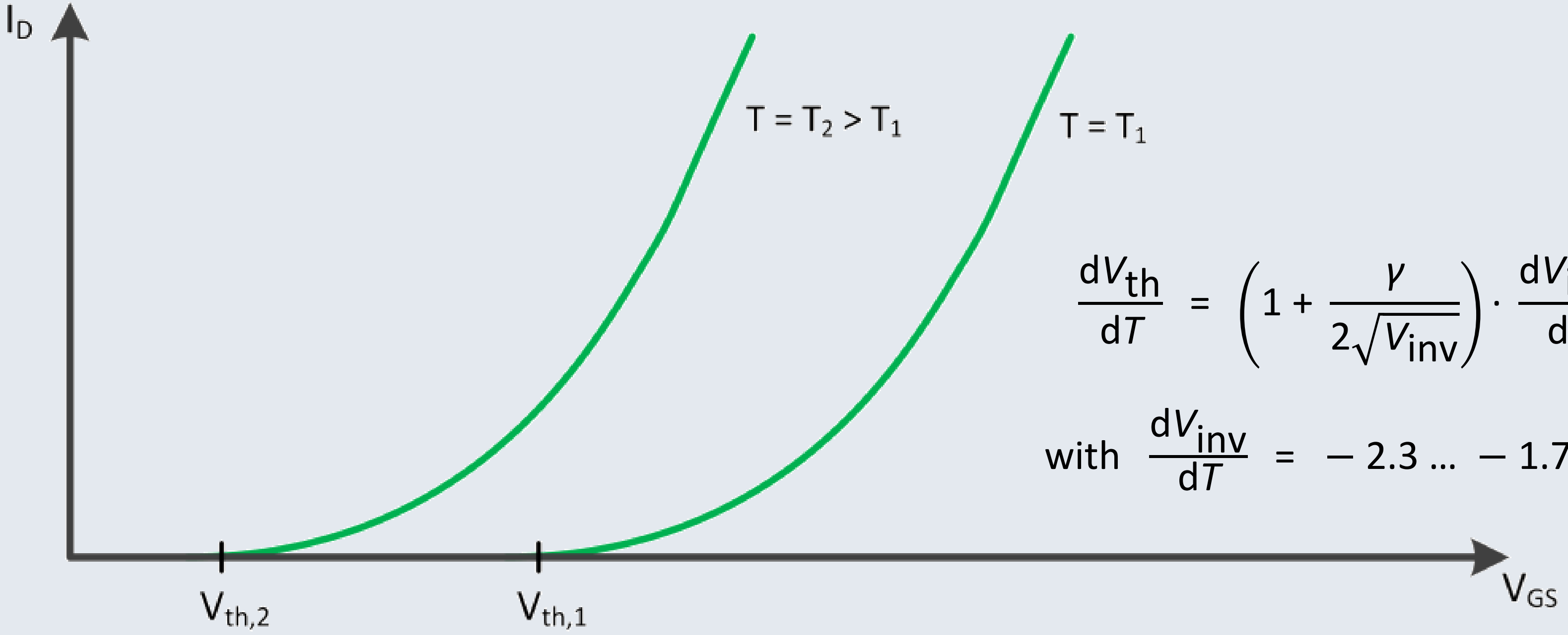
- Only certain pairs of operating points can be reached with this circuit



Gate Bias Circuit

Temperature Compensation

- The threshold voltage of a MOSFET decreases with increasing temperature → the quiescent drain current increases.



$$\frac{\mathrm{d}V_{\mathrm{th}}}{\mathrm{d}T} = \left(1 + \frac{\gamma}{2\sqrt{V_{\mathrm{inv}}}}\right) \cdot \frac{\mathrm{d}V_{\mathrm{inv}}}{\mathrm{d}T}$$

$$\text{with} \quad \frac{\mathrm{d}V_{\mathrm{inv}}}{\mathrm{d}T} = -2.3 \ldots -1.7 \ \frac{\mathrm{mV}}{\mathrm{K}}$$

- The operating point shifts as the device heats up.

Gate Bias Circuit

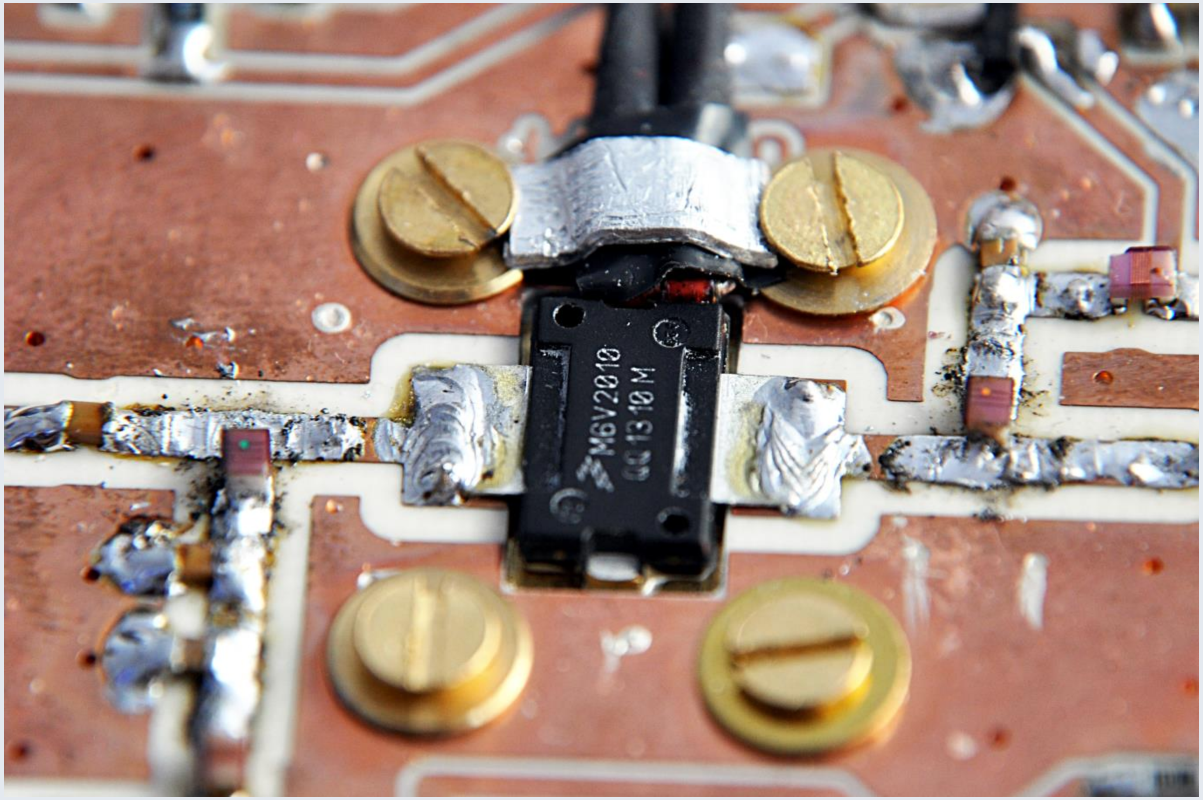
Temperature Compensation

- The forward voltage V_D of a silicon pn–diode follows a similar law as the threshold voltage of a MOSFET: $\frac{dV_D}{dT} \approx -1.7\ \frac{\text{mV}}{\text{K}}$
- Compensation principle:
  - one pn–diode is placed far away from the MOSFET (approximately ambient temperature)
  - one pn–diode is placed close to the MOSFET (approximately junction temperature)
  - The difference between the forward voltages is amplified and added to the selected gate bias voltage by a differential amplifier with common mode offset input of type AD8137

Gate Bias Circuit

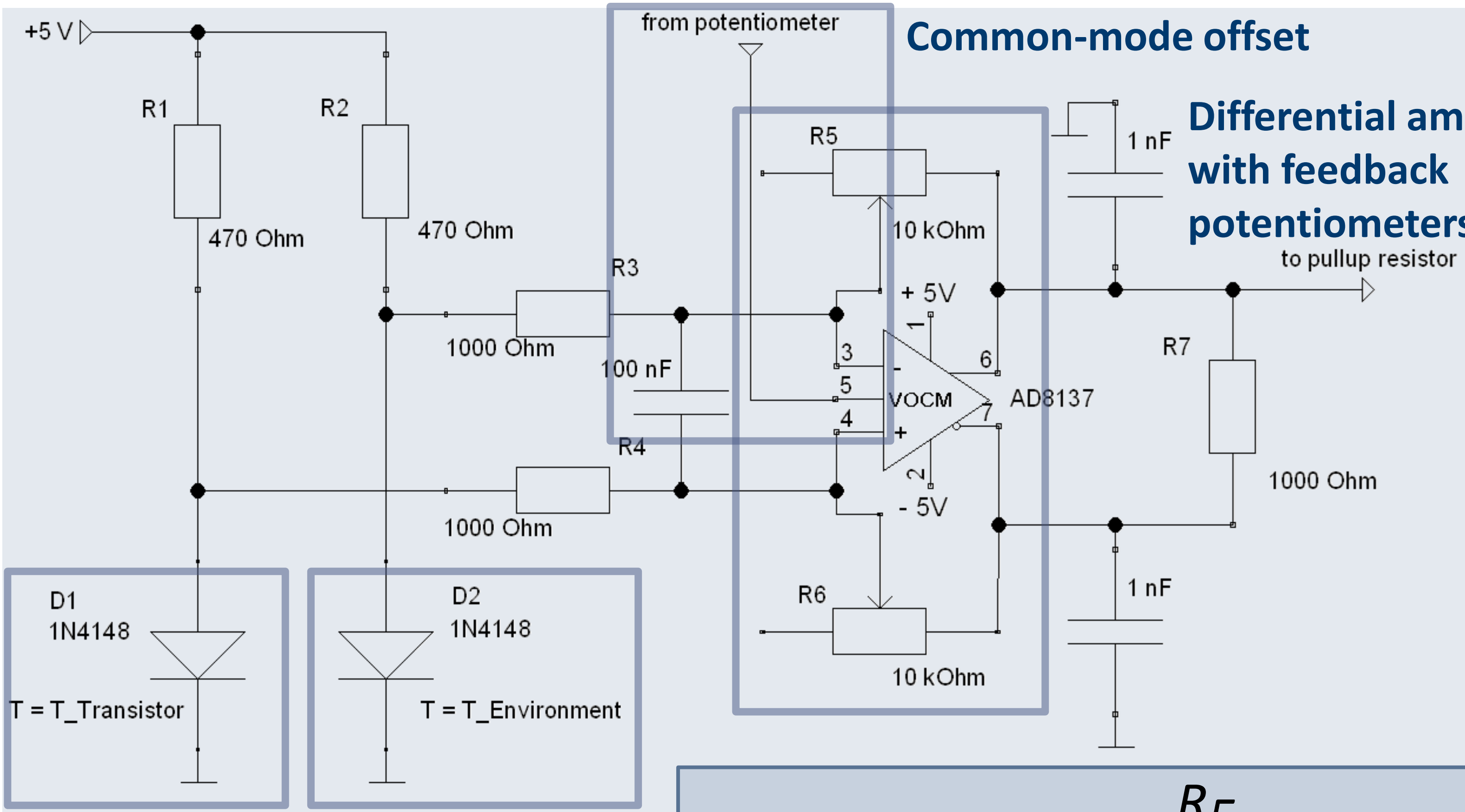
Temperature Compensation

- Sensor diode is placed next to the MOSFET, not on top because diode picks up electromagnetic field radiated by the MOSFET



Gate Bias Circuit

Temperature Compensation



Common-mode offset

Differential amplifier with feedback potentiometers

Temperature sensing diode

Reference diode

$$V'_{\text{Bias}} = V_{\text{Bias}} + \frac{R_5}{R_3} \cdot (V_{\text{D1}} - V_{\text{D2}})$$

Gate Bias Circuit

Temperature Compensation

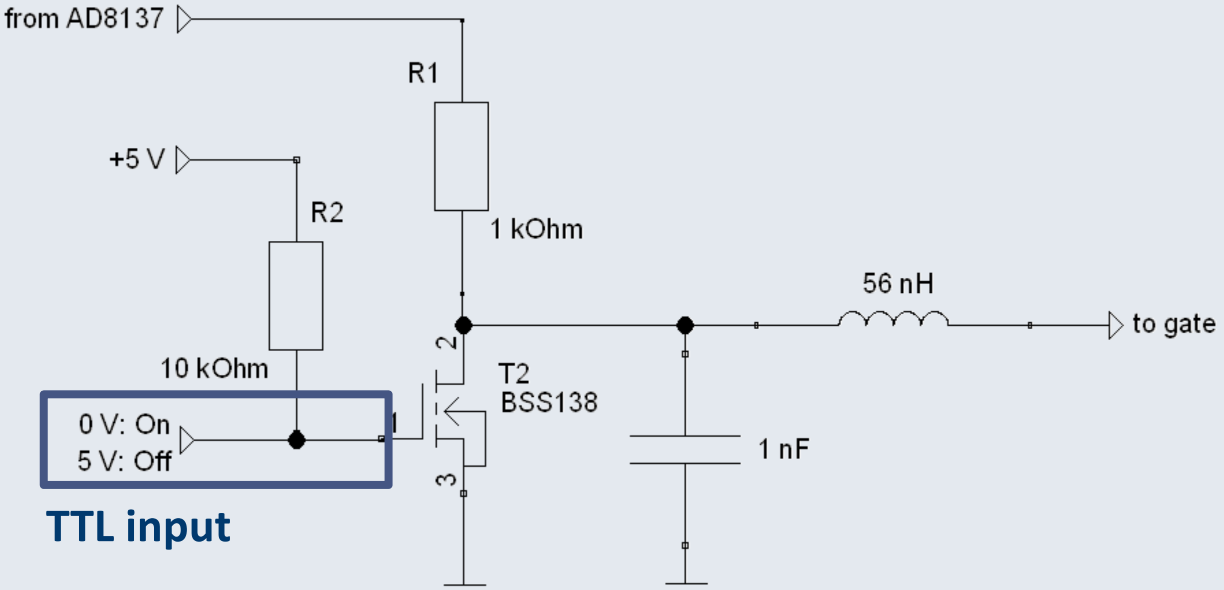
- The feedback potentiometers around the differential amplifier must be set to the same value for the common mode offset to work properly
- A procedure for adjusting the feedback resistors for optimum temperature compensation has been developed.
- The quiescent drain current is held constant to within about 10 mA.
- Problem: In an enclosure the reference diode will eventually heat up, too.

Gate Bias Circuit

On–Off Switching

- Pulsed operation: amplifier does not need to be in its operating point when no pulse is present at the RF input

→ Power dissipated in the MOSFET can be reduced by switching V_{GS} to 0 V between the pulses.



Voltage Regulator

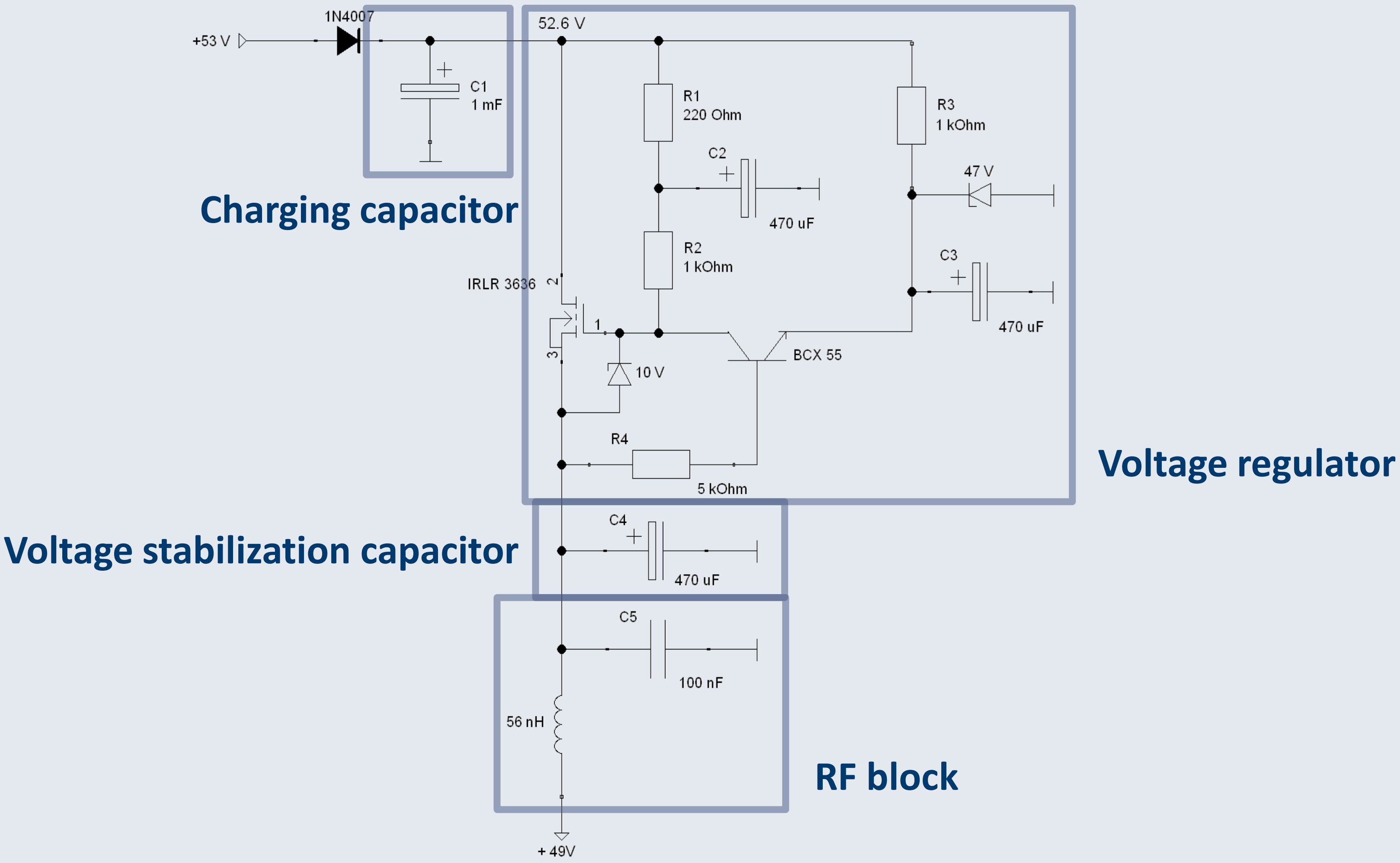
Concept

- Power amplifier needs stable drain–source voltage, especially during the RF pulses
- Little current flowing into the drain between the pulses
- Significant current flowing into the drain during the pulses
  - Large transients
  - Power supply regulator is under stress
  - Power line inductance hinders transients
  - Power supply might not be able to provide the required drain current

→ **Solution:** charging capacitors and discrete voltage regulator close to the amplifier

Voltage Regulator

Circuit



Charging capacitor

Voltage regulator

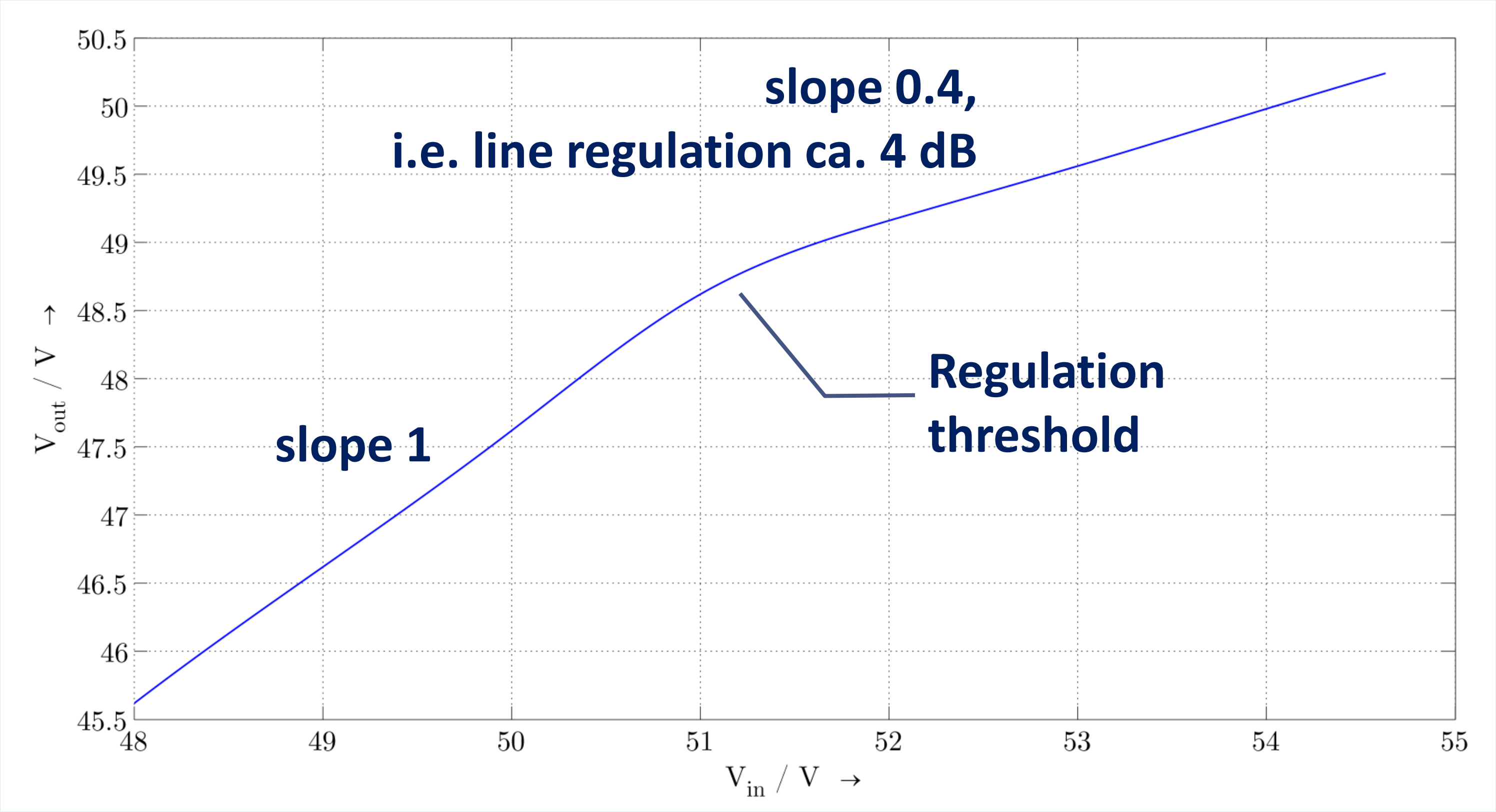
Voltage stabilization capacitor

RF block

Voltage Regulator

Static Line Regulation

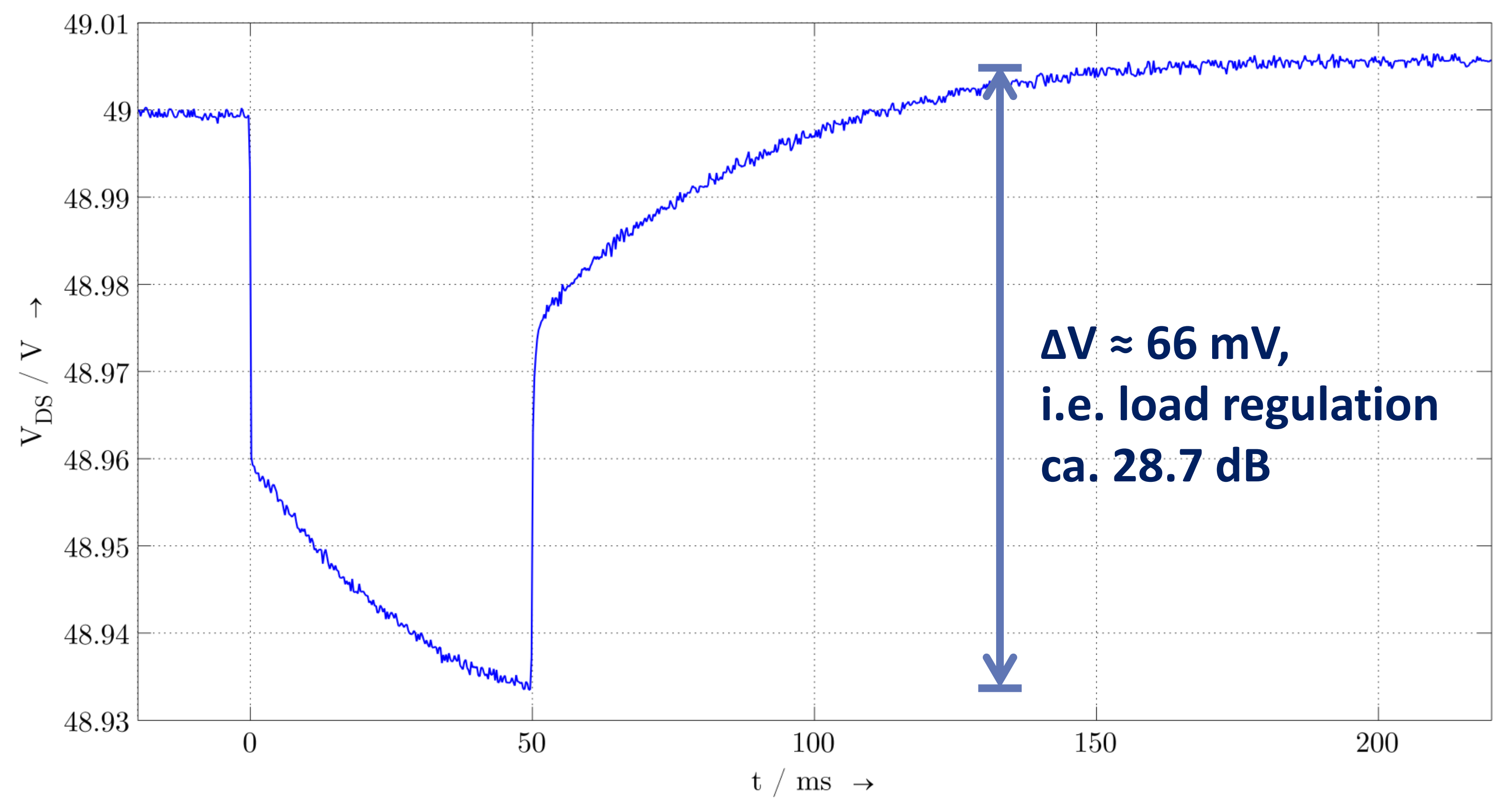
- Static line regulation: dependence of the output of a regulator on the input in the static case



Voltage Regulator

Load Regulation

- Load regulation: dependence of the output of a regulator on the load



**ΔV ≈ 66 mV,
i.e. load regulation
ca. 28.7 dB**

Power Monitor

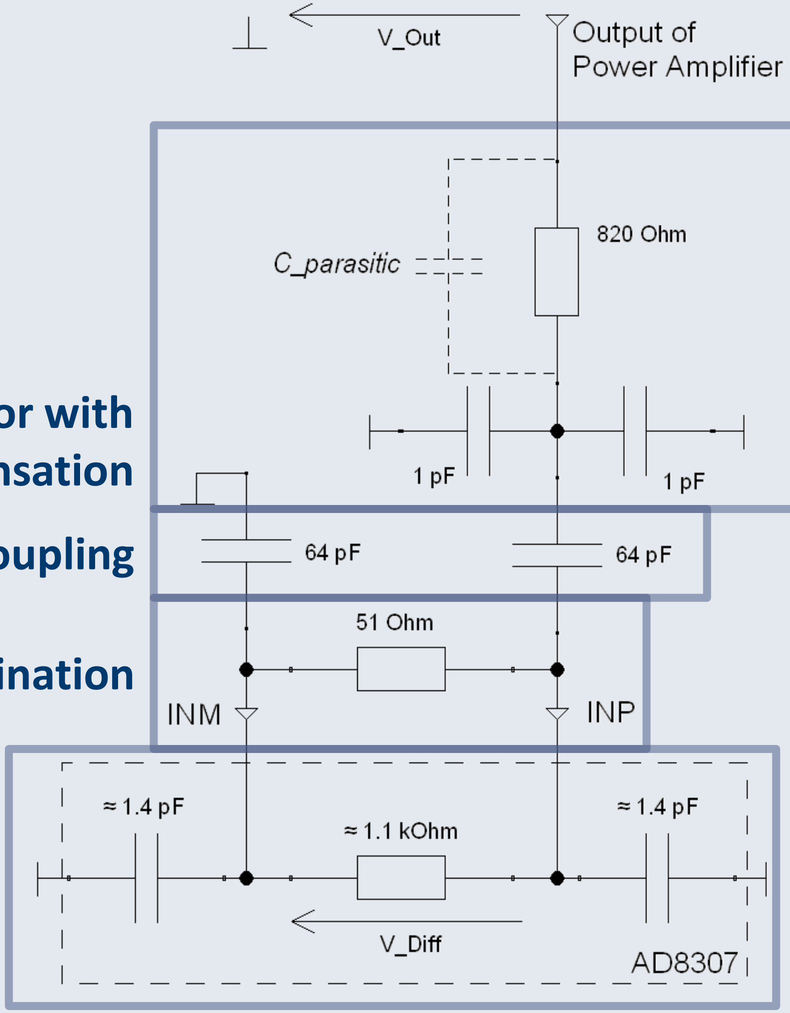
Concept

- Necessity to measure the output power of the amplifier during operation
- Difficult because of high frequency and large dynamic range
- Solution: AD8307 logarithmic amplifier
    - converts RF voltage to d.c. voltage (envelope)
    - outputs a voltage that is proportional to the logarithm of the input voltage
- Theoretically output power can be measured with a multimeter this way

Power Monitor

Concept

- Output voltage of the driver amplifier needs to be reduced to within the input range of the AD8307 with a probe circuit



Probe resistor with frequency compensation

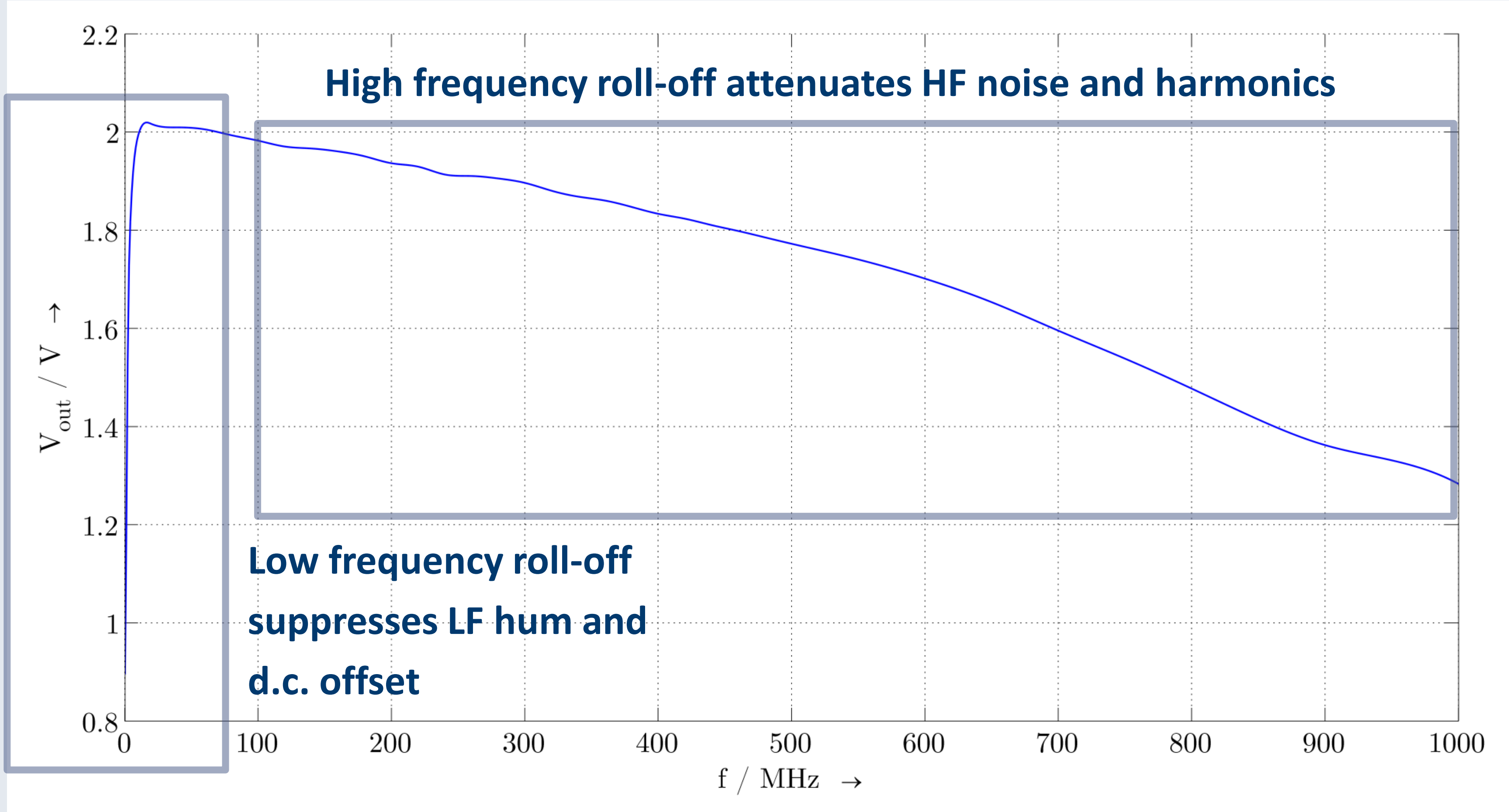
a.c. coupling

50 Ω termination

Input equivalent circuit of the AD8307

Power Monitor

Frequency Response

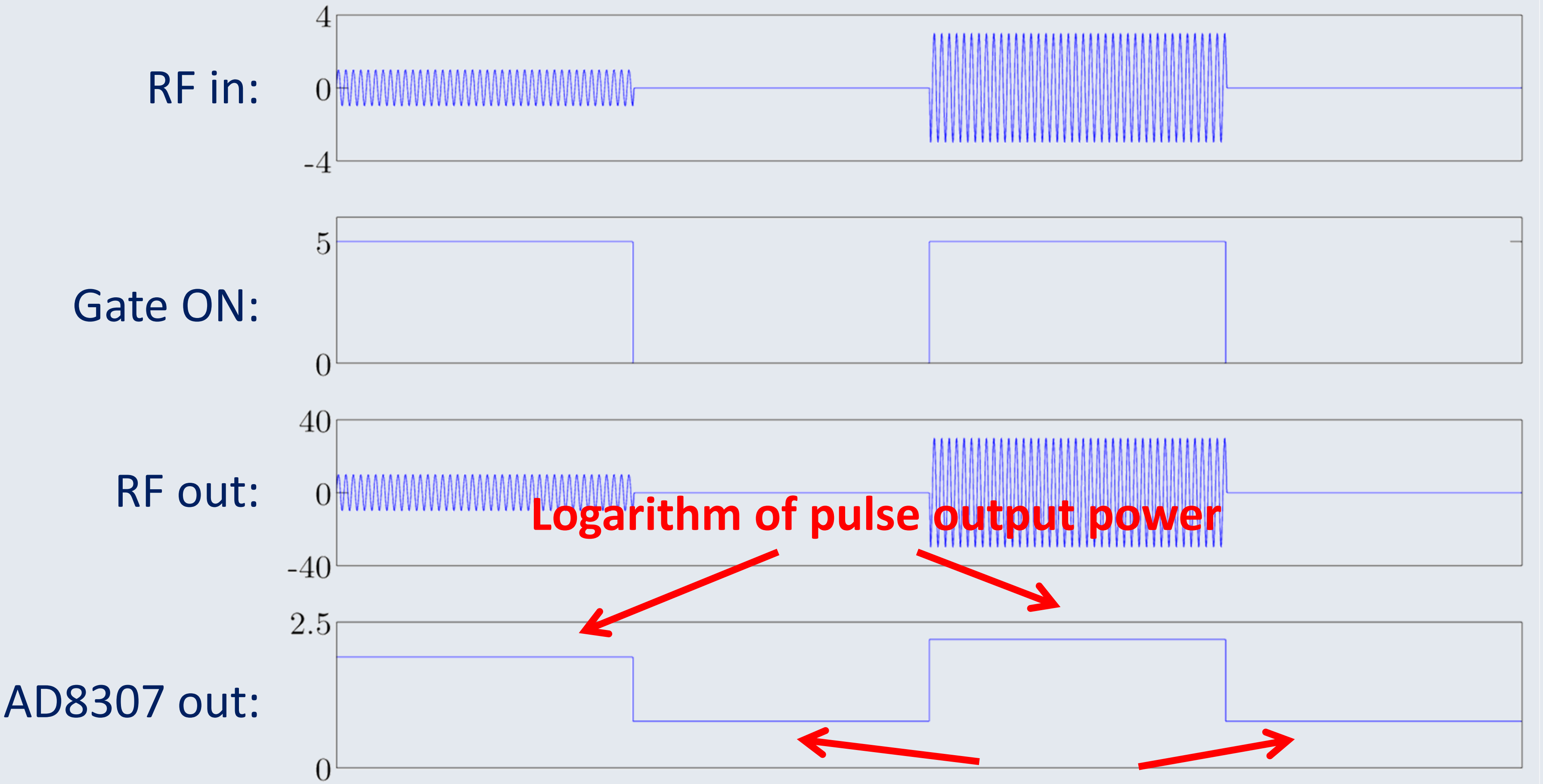


High frequency roll-off attenuates HF noise and harmonics

Low frequency roll-off suppresses LF hum and d.c. offset

Power Monitor

Pulsed Operation



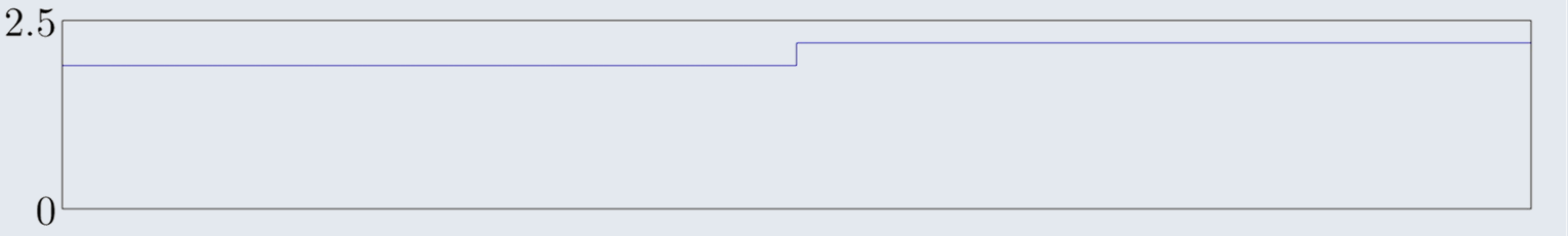
Logarithm of pulse output power

Logarithm of noise power

Power Monitor

Sample–and–Hold Circuit

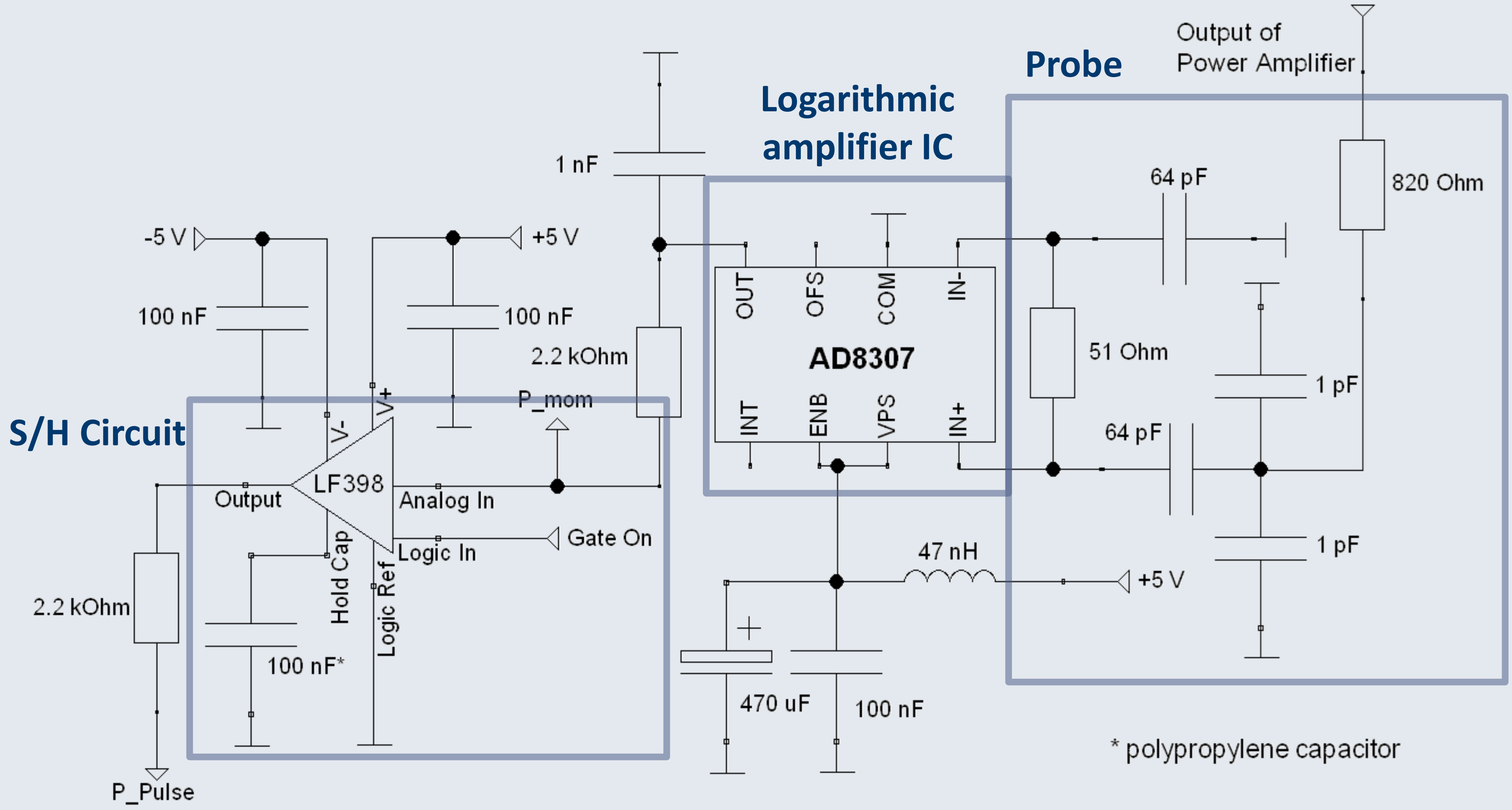
- Consequence for measurement of output power:
  - Analog multimeter: approx. measures average power
  - Oscilloscope: measures pulse and noise power
  - Digital multimeter: does not allow any sensible measurement
- Solution: Sample–and–hold circuit based on an LF398 that holds the output voltage of the AD8307 between the pulses



- S/H circuit can be controlled by “Gate ON” voltage because it is supposed to be high only during the RF pulses

Power Monitor

Complete Circuit



Logarithmic amplifier IC

Probe

S/H Circuit

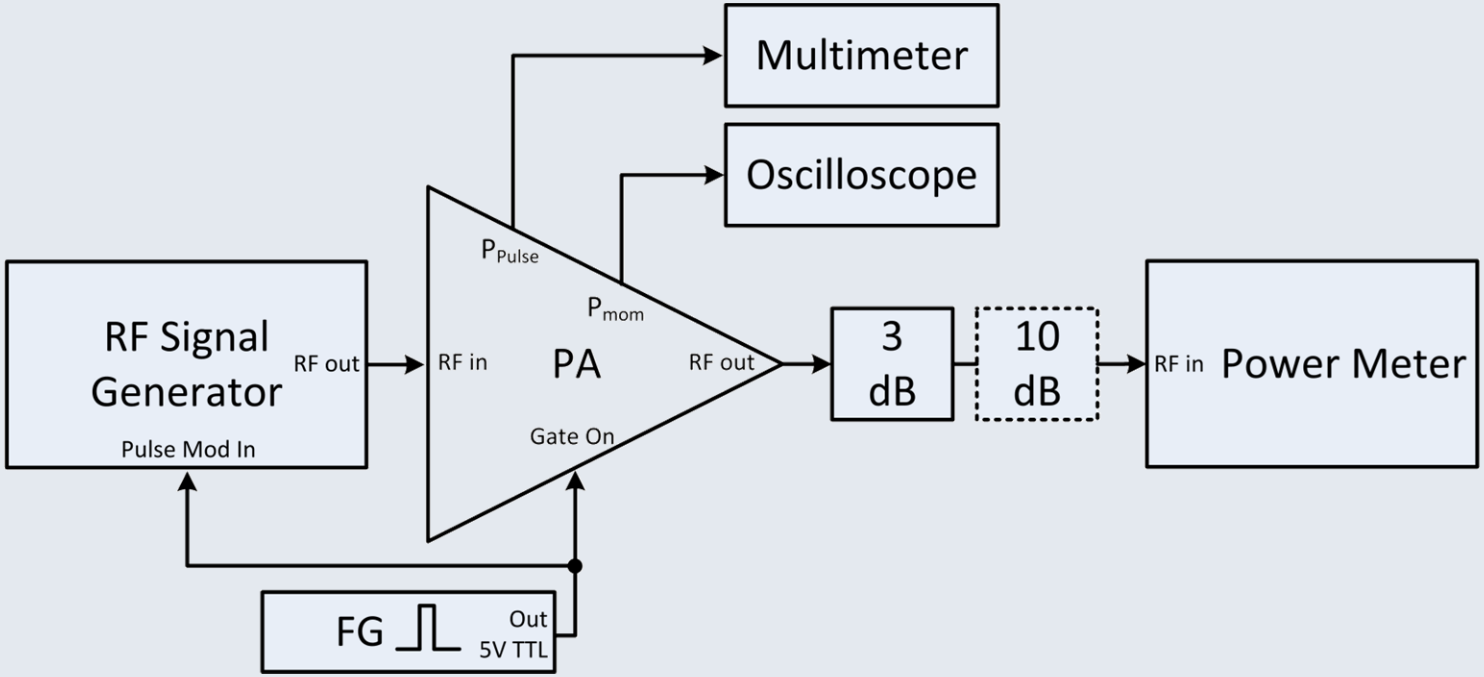
* polypropylene capacitor

Power Monitor

Calibration

- Relationship between d.c. output voltage and output power must be established

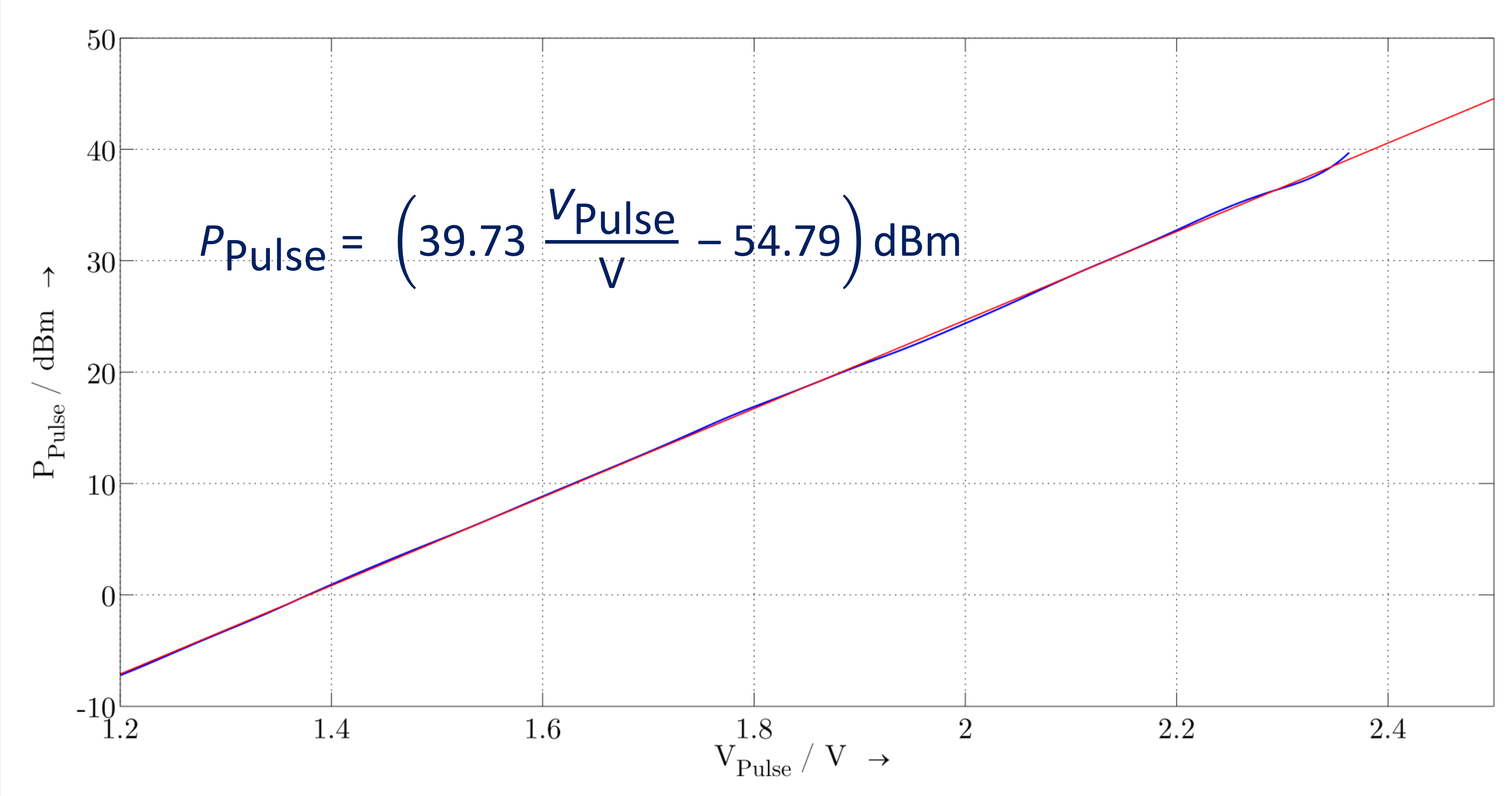
→ Calibration against a reference power meter



Power Monitor

Calibration

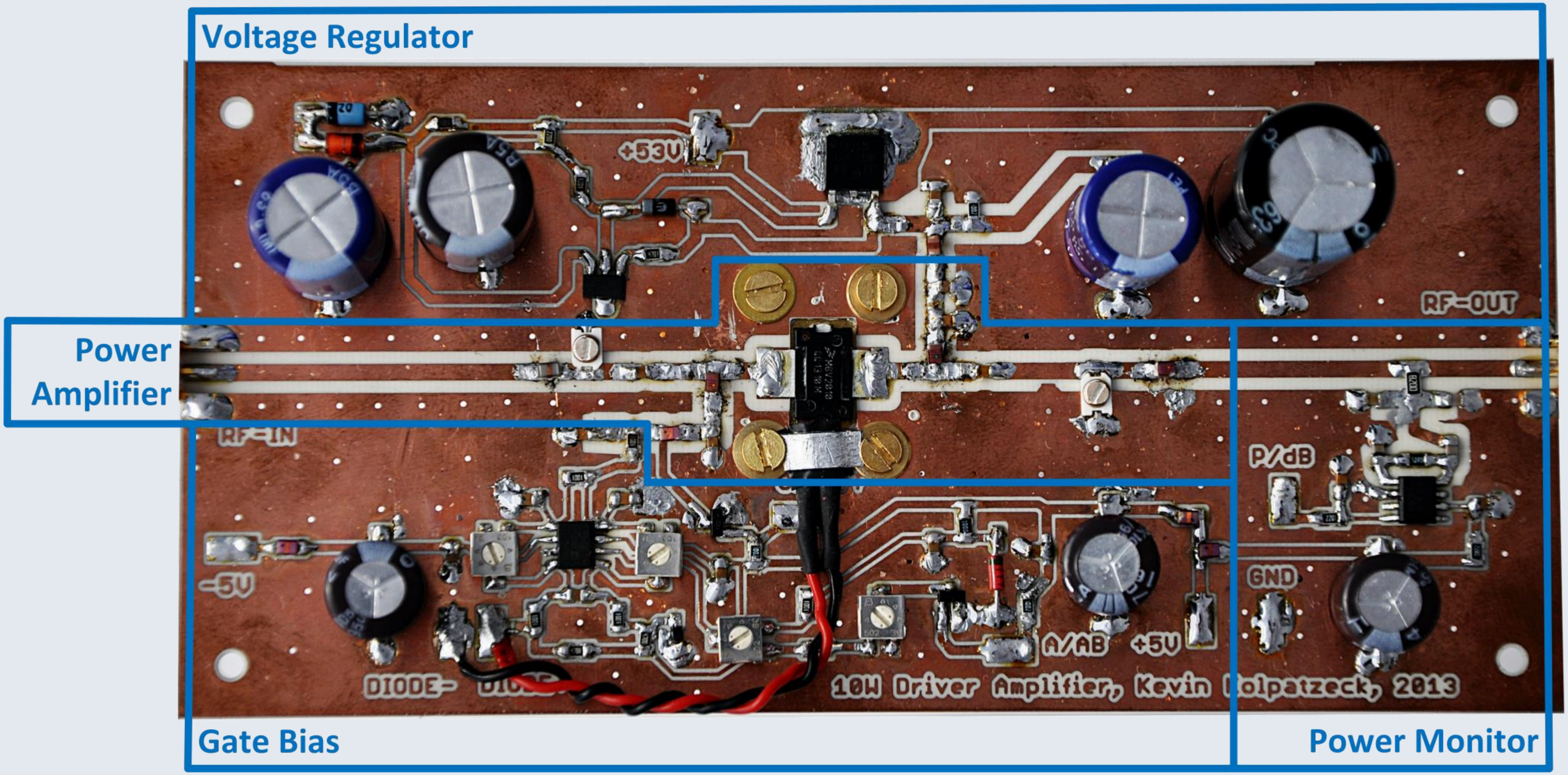
- Linear law between d.c. output voltage and power in dBm:



$$P_{\mathrm{Pulse}} = \left(39.73\,\frac{V_{\mathrm{Pulse}}}{\mathrm{V}} - 54.79\right)\mathrm{dBm}$$

Assembly

Circuit Board Layout

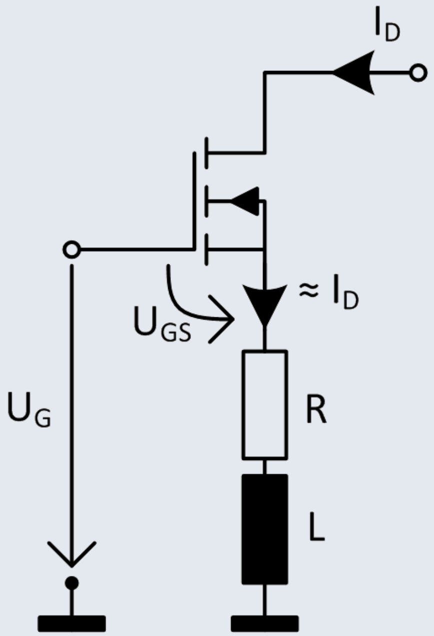


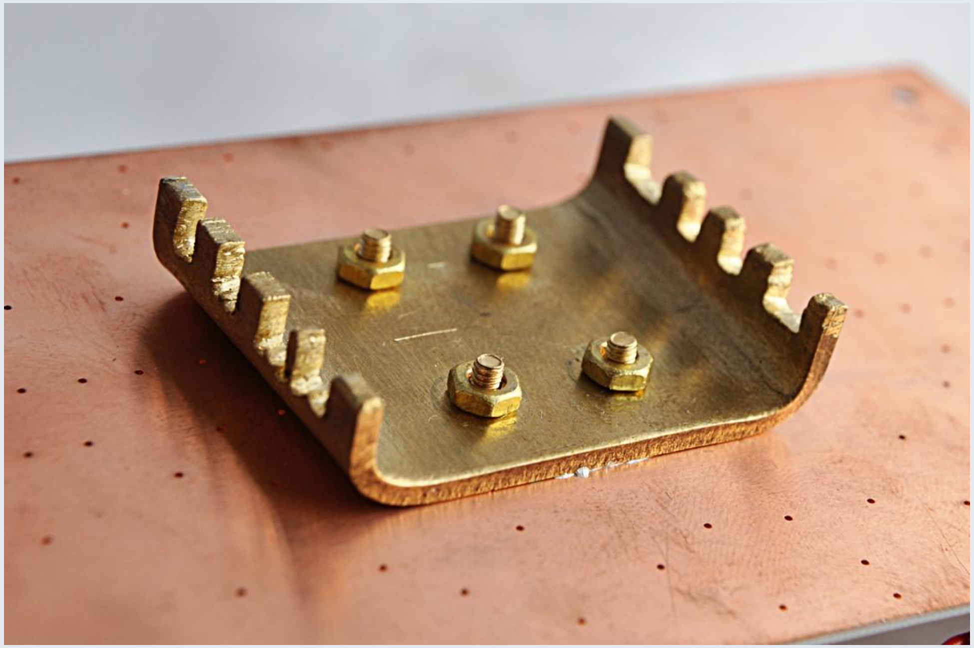
Assembly

Power MOSFET Mounting

- Good source–ground connection (low resistance, low inductance) and low thermal resistance is important

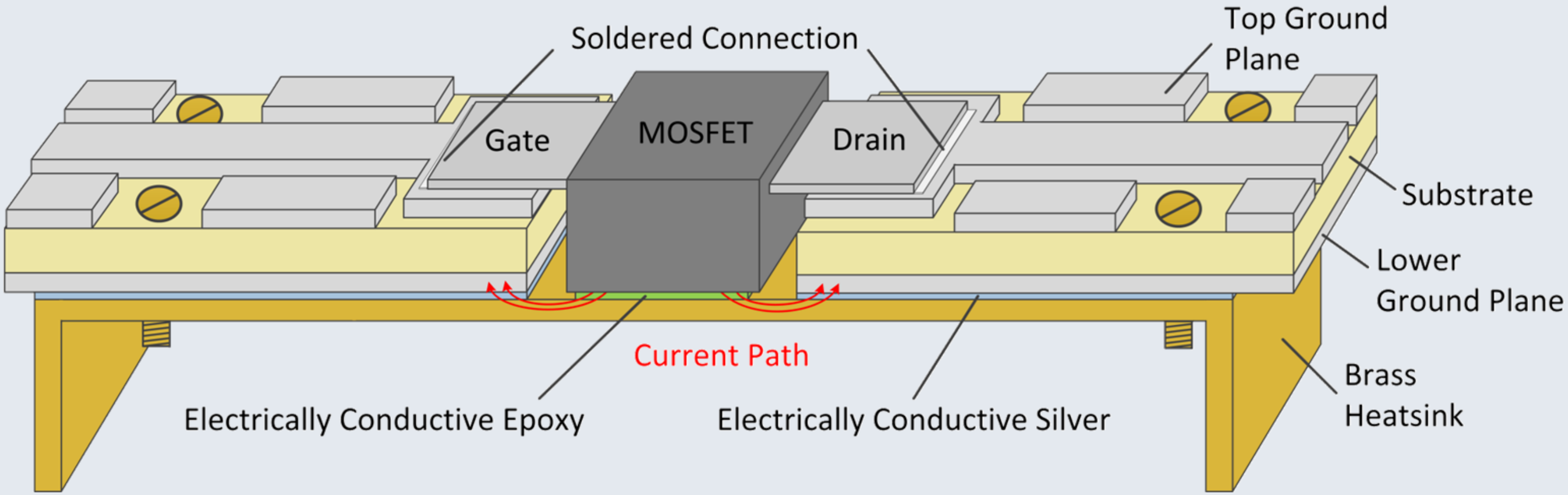
→ Glue–on mounting on a self–built brass heatsink





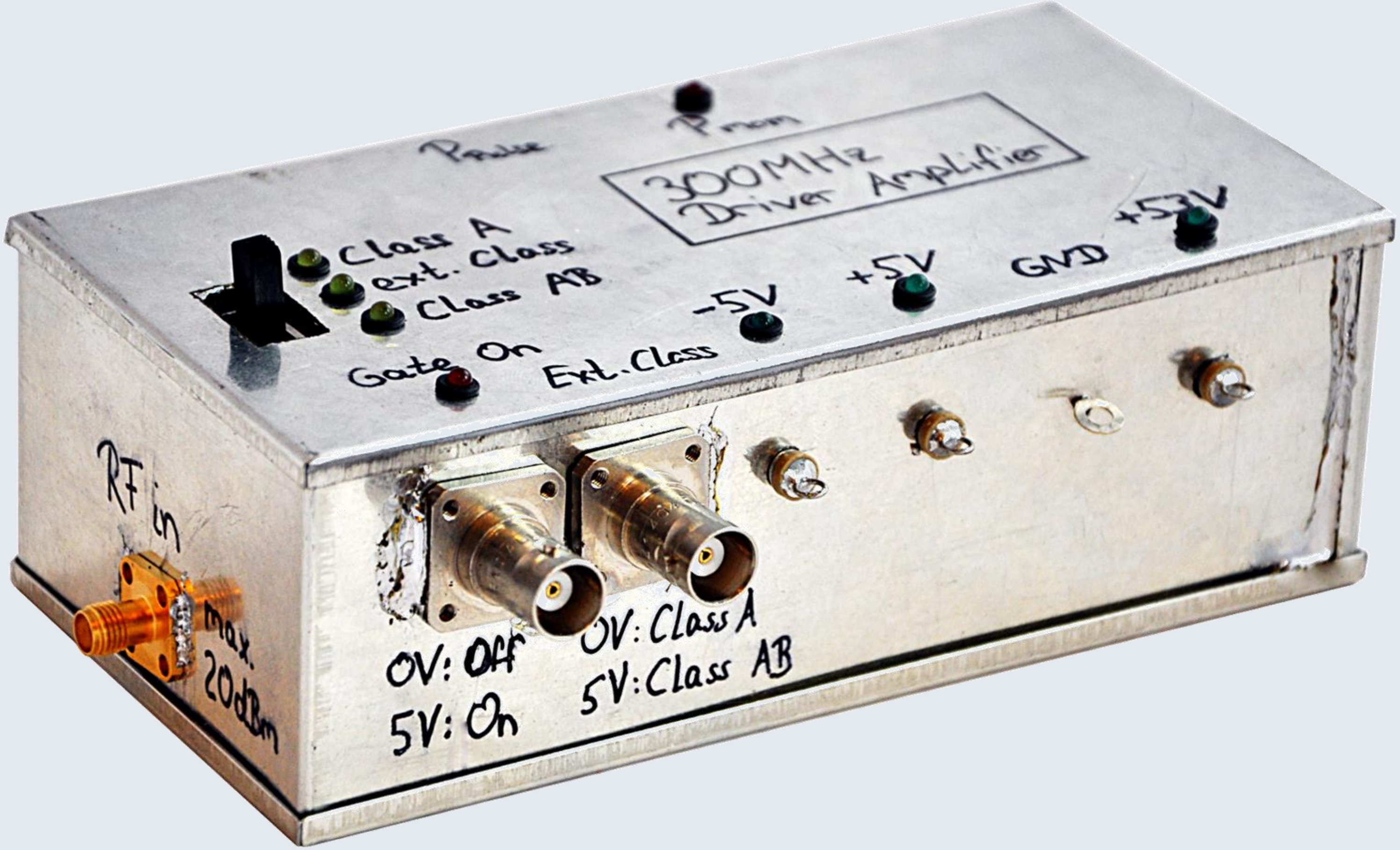
Assembly

Power MOSFET Mounting



Assembly

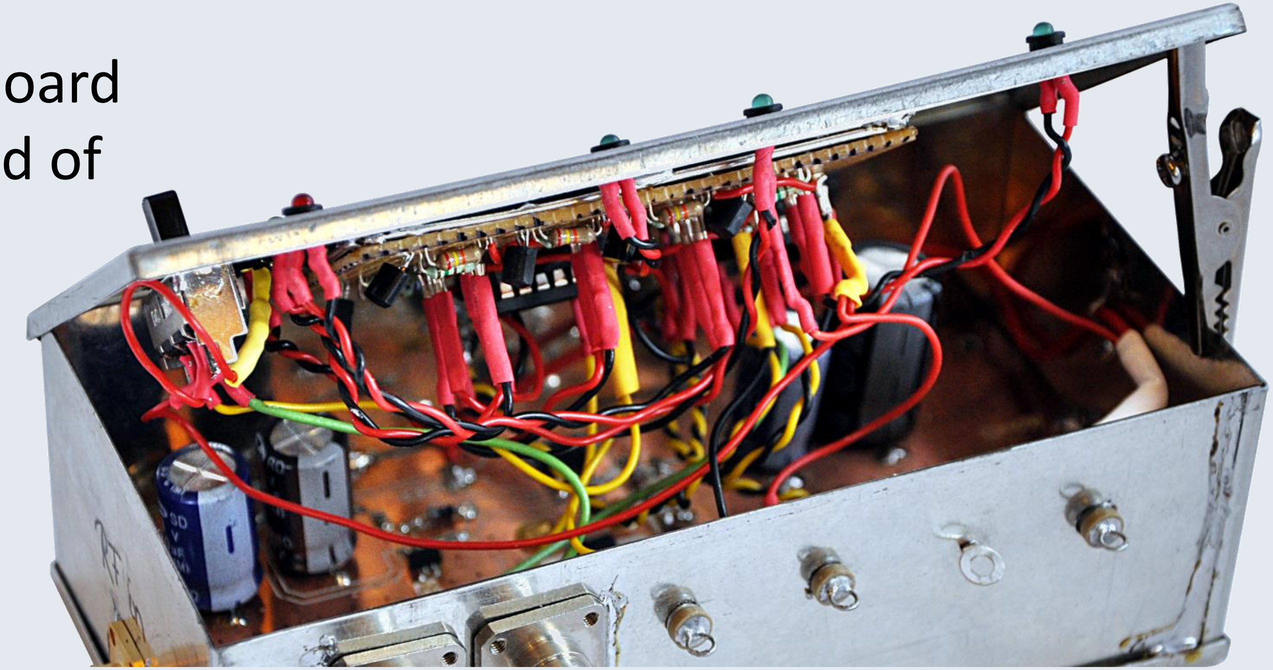
Housing



Assembly

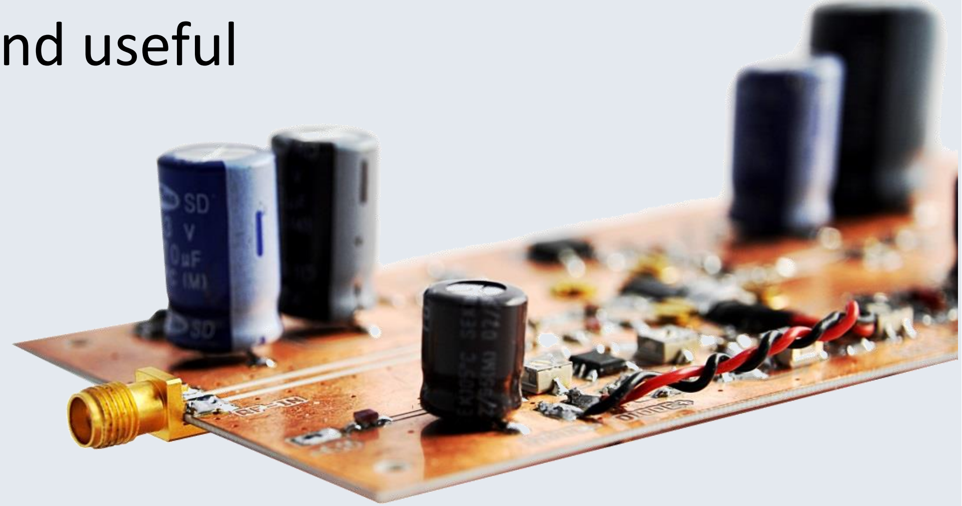
Additional Circuitry

- Signaling LEDs
- Inverter for the Gate ON voltage
- Polarity protection
- Placed on a perfboard underneath the lid of the box



Conclusion

- Complete, conveniently usable amplifier for amplification from 100 mW to 10 W
- Amplification and maximum output power higher than expected
- Relatively poor distortion figures
- Concepts for use in driver and high power amplifier have been tested and proven functional and useful
  - Operating point flexibility
  - Temperature compensation
  - Gate shutdown
  - Power Monitor



Thank you for your interest!