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HFT

Design of a Test Interface Unit for Switch/Modulator Cassette in 7 Tesla MRI System

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DTIU-Outlet

- **Introduction**

  Looking Through of whole Test System
- **Working Principle of the Circuit under Test**

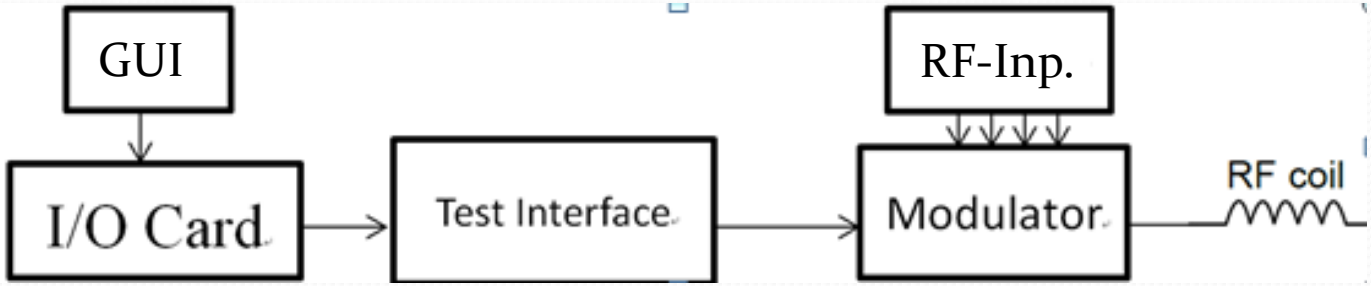
  Digital to Analog Converter(DAC) MAX5100

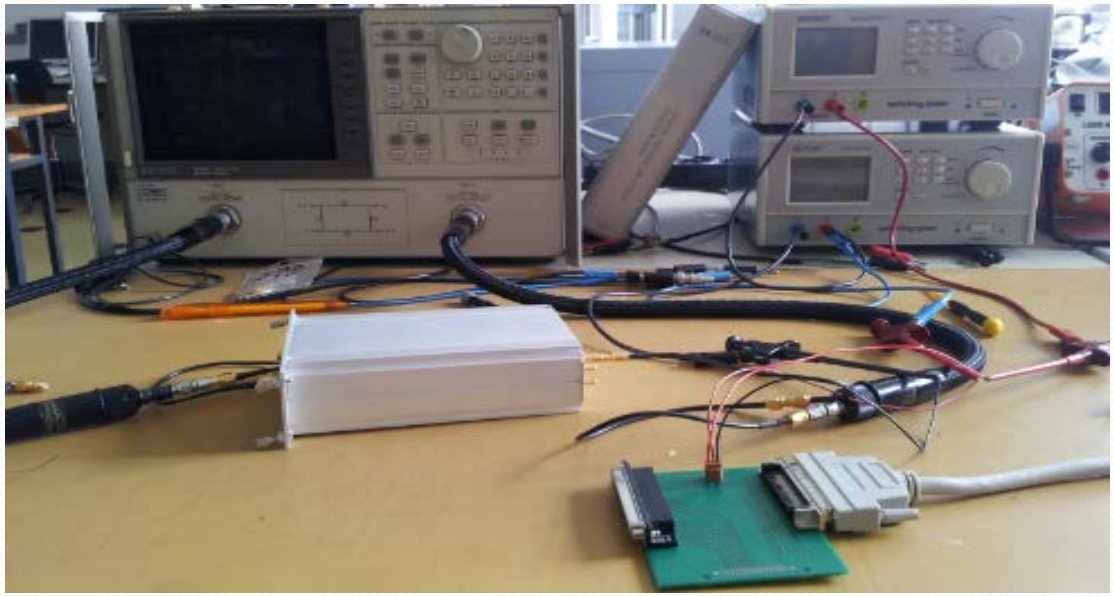
  Process of test
- **Design of the Printed Circuit Board (PCB)**

  Connected-condition of 3 different Connectors

  Principle of “Quancom” I/O Card
- **Design of the Graphical User Interface (GUI)**
- **Test Results**

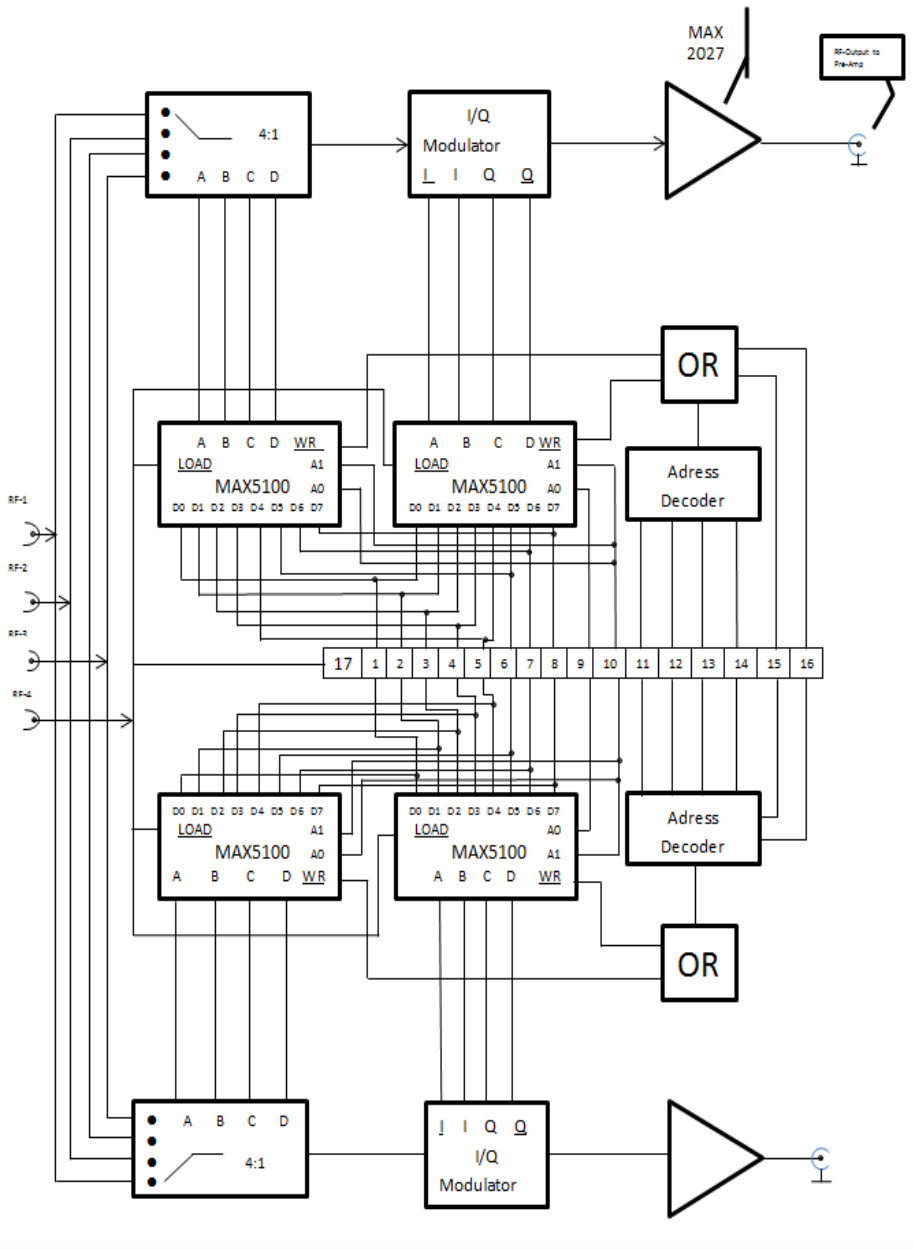
DTIU-Looking through of whole Test System



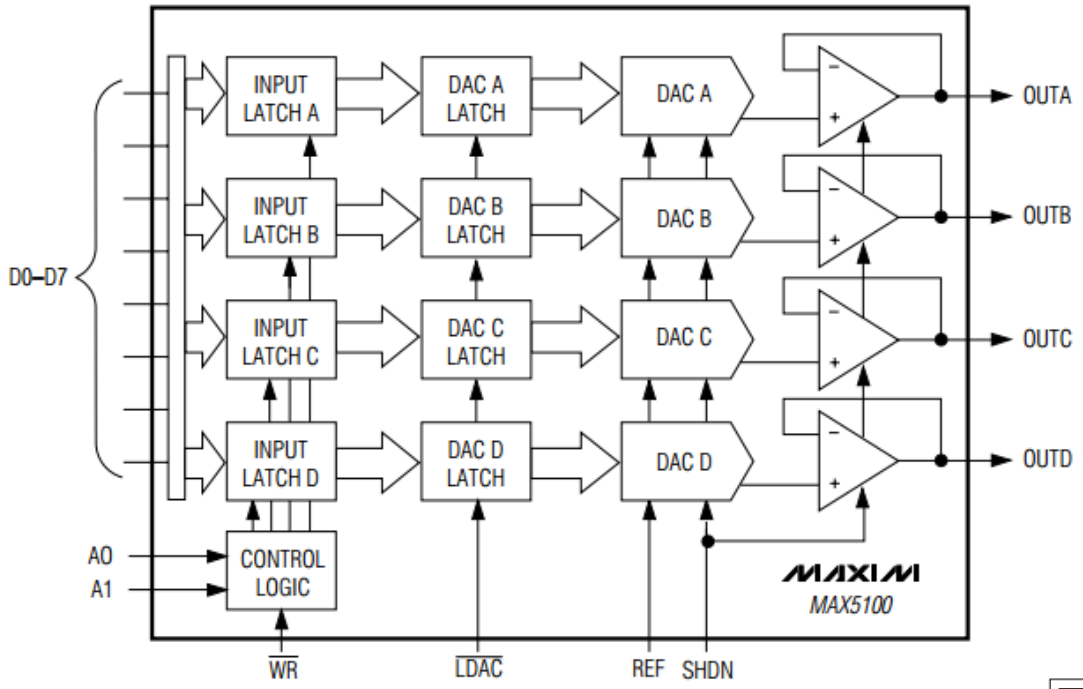


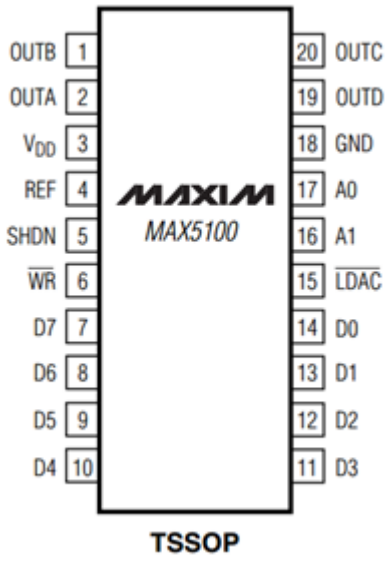
DTIU-Working Principle of the Circuit under Test

- Bit 1-8 : Data bits
- Bit 9-10 : Address bits of DAC in Switch/Modulator
- Bit 11-14 : Address bits of cassette
- Bit 15 : Contorl bit of switch and modulator
- Bit 16 : Control bit of data writing
- Bit 17 : Control bit of the outputs transparent



DTIU-Digital to Analog Converter(DAC)





	Bit 9	Bit 10
Output A	1	0
Output B	0	0
Output C	0	1
Output D	1	1

LDAC	WR	A1	A0	LATCH STATE
H	H	X	X	Input and DAC data latched
H	L	L	L	DAC A input latch transparent
L	H	X	X	All 4 DACs' DAC latches transparent
L	L	L	L	DAC A input registers transparent and all 4 DACs' DAC latches transparent
H	L	L	H	DAC B input latch transparent
H	L	H	L	DAC C input latch transparent
H	L	H	H	DAC D input latch transparent

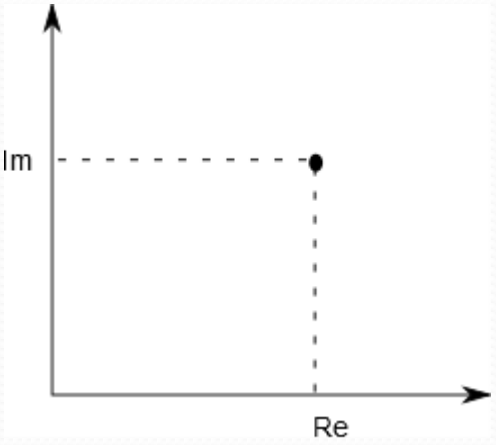
H = High state, L = Low state, X = Don't care

DTIU-DAC for Modulator

- Vout = $(N_B \cdot U_{REF}) / 256$

Output A	Output B	Output C	Output D
$\underline{I}$	I	Q	$\underline{Q}$

- Re = I - $\underline{I}$ Im = Q - $\underline{Q}$



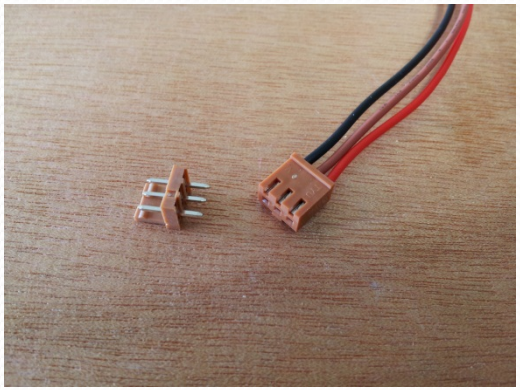
DTIU-DAC for RF-Input Switch

RF-Input Port	Output A/Logic	Output A/Logic	Output A/Logic	Output A/Logic
1	1	0	1	1
2	0	1	1	1
3	1	1	1	0
4	1	1	0	1

Voltage Level for logic 1 is 5 V and for logic 0 is 0V

DTIU-Components of the PCB

68 Pins D-Sub Connector



3 Poles Power Jack

37 Pins D-Sub Connector

68 Pins Very-high-density cable interconnector

DTIU-Voltage Level Standard of I/O Card

- Pin Configuration of the Card's 68 Pins

Pin Num.	1-32	33-34	35-66	67-68
Pin Conf.	I/O 1-32	GND	I/O 33-64	3.3V

- Transistor-Transisitor Logic(TTL) Standard

Logic conditon	High State	Low State	Initial State
Digital Value	1	0	--
Voltage Range	>=2.4V	<=0.4V	0.8V<=U<=2.4 V
Voltage	3.6V	0V	1.2V

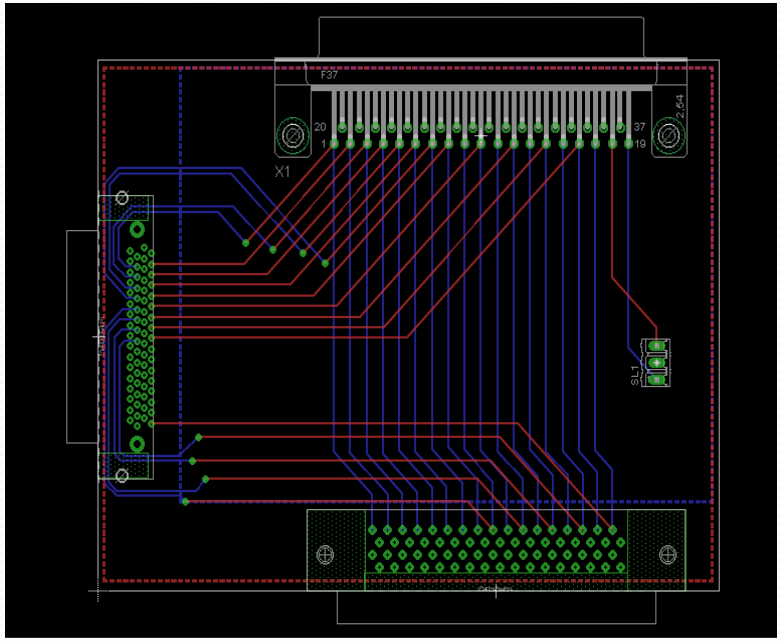
DTIU-Correponding connect-relation for 3 Connectors

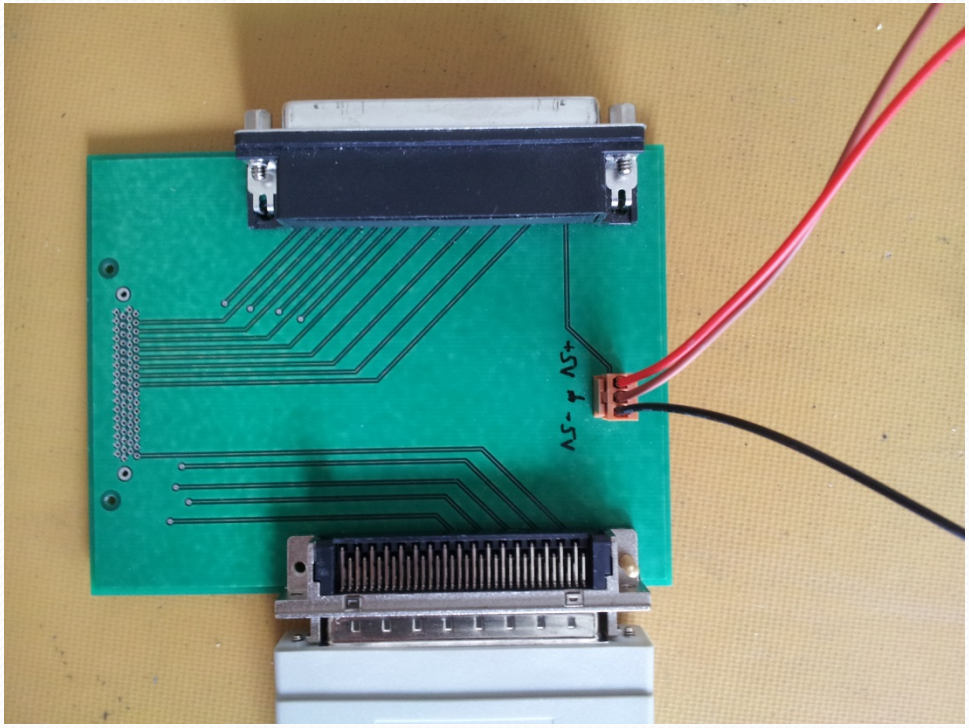
Logic Bits	1	2	3	4	5	6	7	8	9
68Pin D-Sub	**31**	32	30	28	26	24	22	20	18
37Pin D-Sub	1	2	3	4	5	6	7	8	9
VHDCI	65	31	63	29	61	27	59	25	57

Logic Bits	10	11	12	13	14	15	16	17	18	19
68Pin D-Sub	16	14	12	10	8	6	4	2	---	---
37Pin D-Sub	10	11	12	13	14	15	16	17	+5V	-5V
VHDCI	23	55	21	53	19	51	17	1	---	---

* VHDCI：Very-high-density cable interconnector

DTIU-Layout and Finished product of PCB

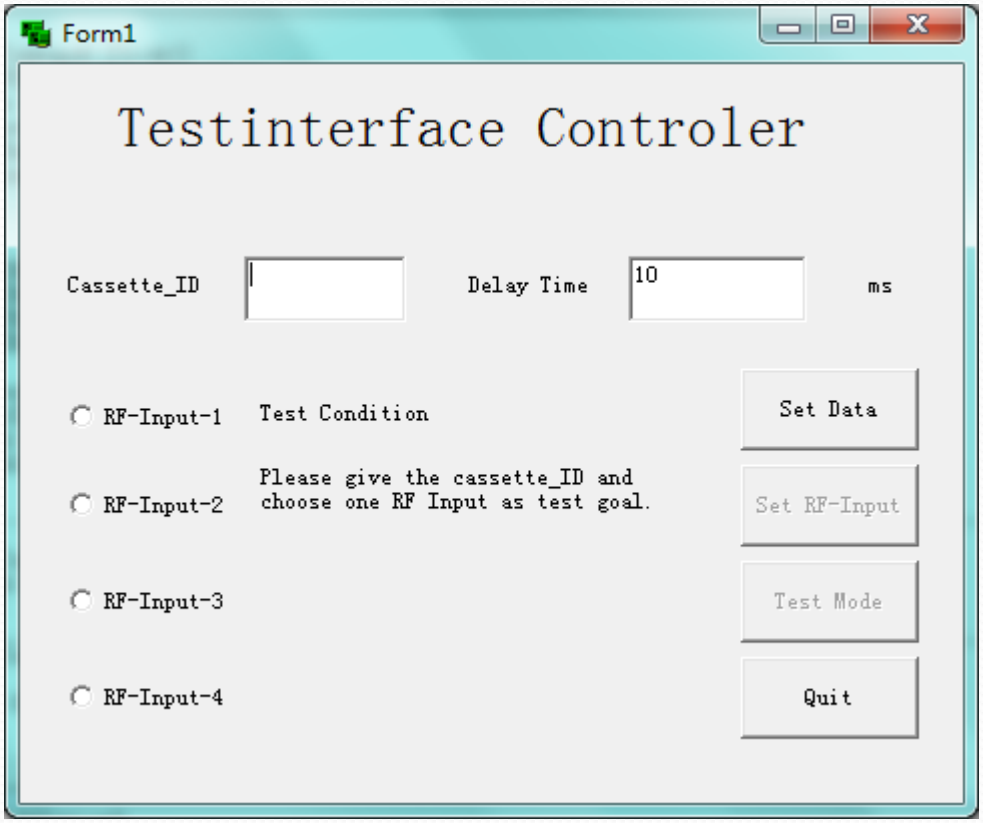


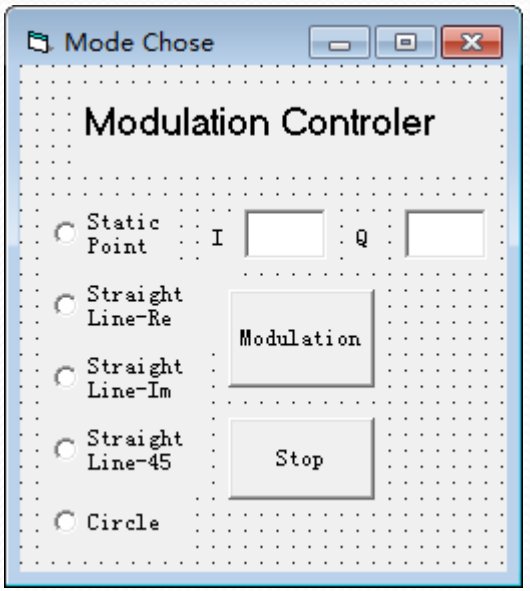


DTIU-Main Functions used in Coding

- *ULONG QAPIExtOpenCard (ULONG cardid, ULONG devnum);*
- *ULONG QAPIExtCloseCard (ULONG cardhandle);*
- *ULONG QAPIExtSpecial (ULONG cardhandle ULONG jobcode ULONG para1 ULONG para2);*
- *void QAPIExtWriteDO1 (ULONG cardhandle ULONG channel ULONG value ULONG mode);*
- **Wait(Long delaytime)**
- **setRfinputID(Long RFID)**
- **Modulation(Long S, Long X)**
- **setModulation1(Long I, Long Q)**
- **setModulation2-5**

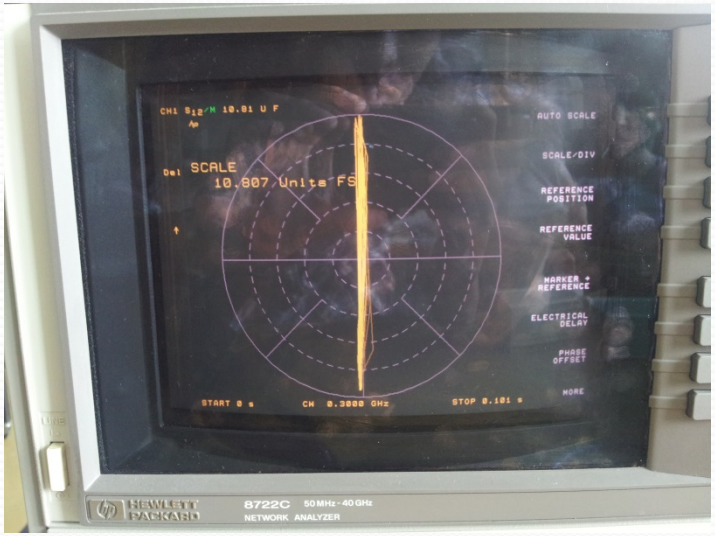
DTIU - Interface and Feature of the GUI

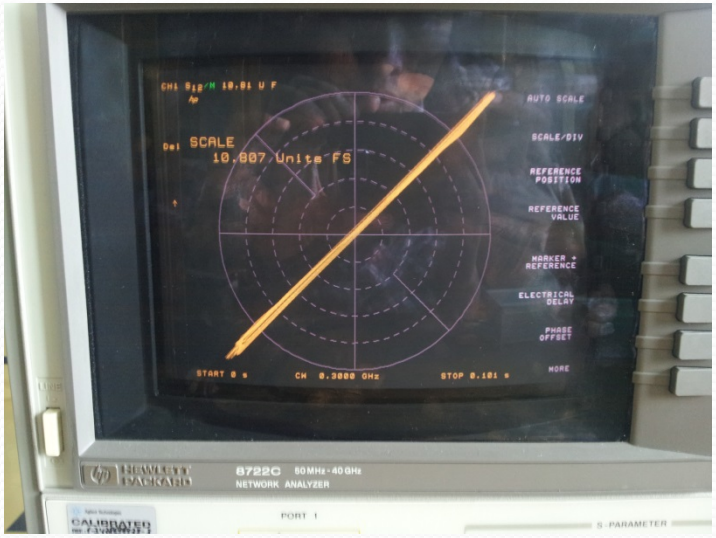


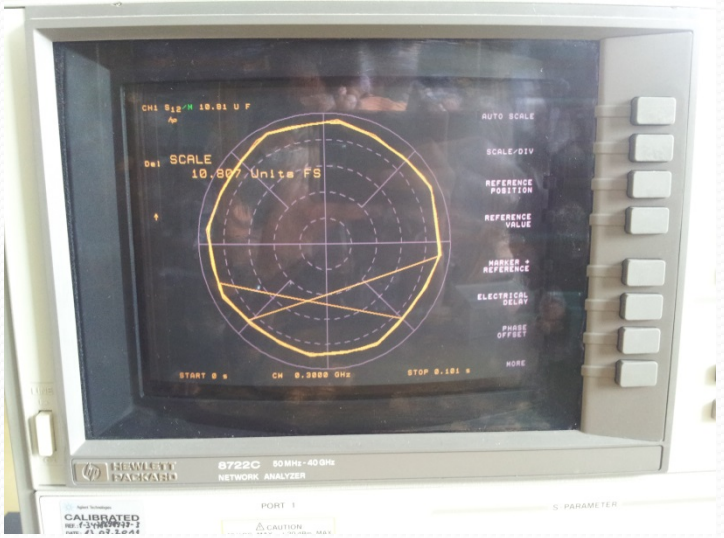


*Maximum Values of Real and Imaginary part of one Point is +/- **3.4V.**

DTIU-Test Result shown in VNA Display







THANK YOU

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