Investigation of Comparator Topologies and their Usage in a Technology Independent Flash-ADC Testbed

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- Introduction
- State-of-the-Art Analog-to-Digital Converters (ADCs)
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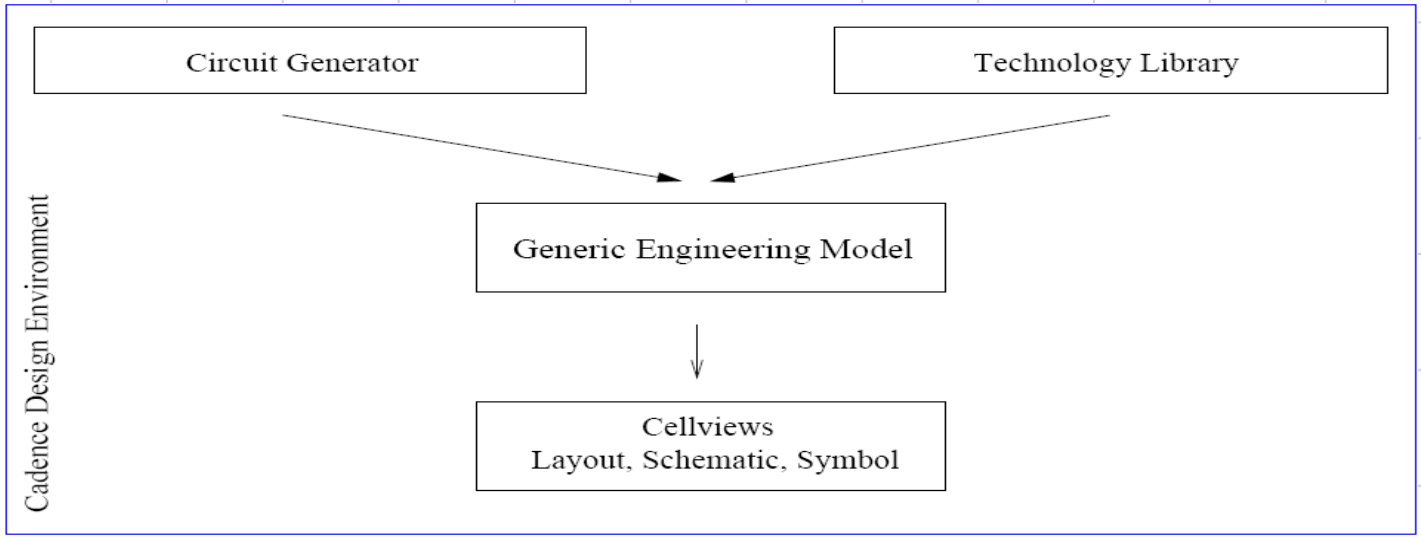
- Comparator Selection Procedure
- Flash ADC Testbed Verification in 65 nm Technology
- Conclusion

Introduction: Generic Engineering Model

- Variety of process technologies increases
- Circuits have to be rebuilt for every process
- The Generic Engineering Model (GEM)
  - Circuits are portable to all technologies
  - Automatical symbol, schematic, layout and testbench generation
- During this thesis, all circuits were developed using the GEM approach



Introduction: Selection methodology

- Selection methodology on top of GEM implementation allows parameterizable layout solutions
- Main high level design constraints:
  - Power
  - Supply voltage
  - Area
  - Bit resolution
  - Speed (clock rate)
- Comparator topologies are investigated with respect to the above listed constraints for flash ADC implementation

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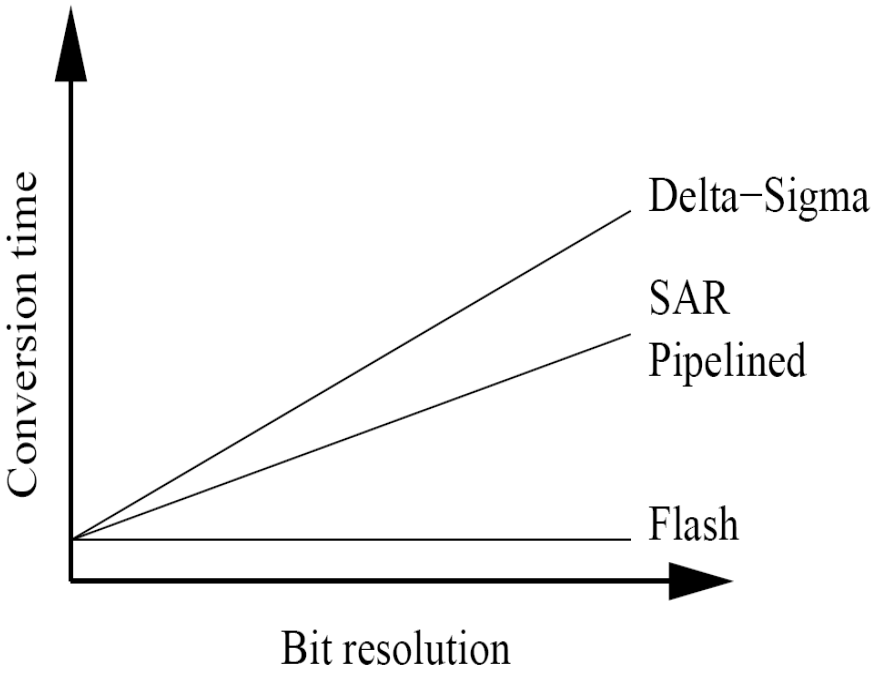
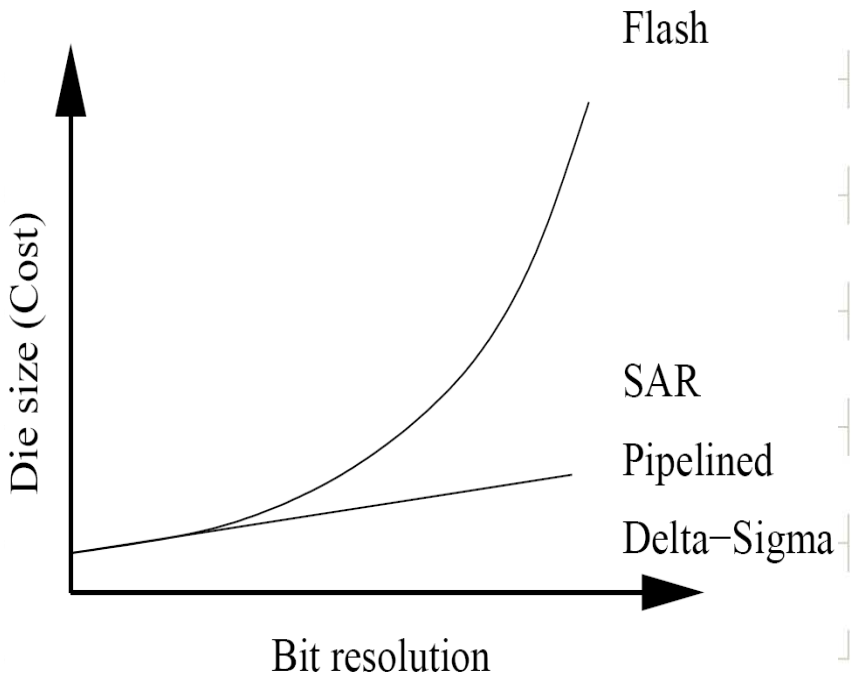
State-of-the-Art ADCs

- ADCs are developed for high speed or high resolution
- High resolution and high speed leads to high die size (high costs and implementation effort)





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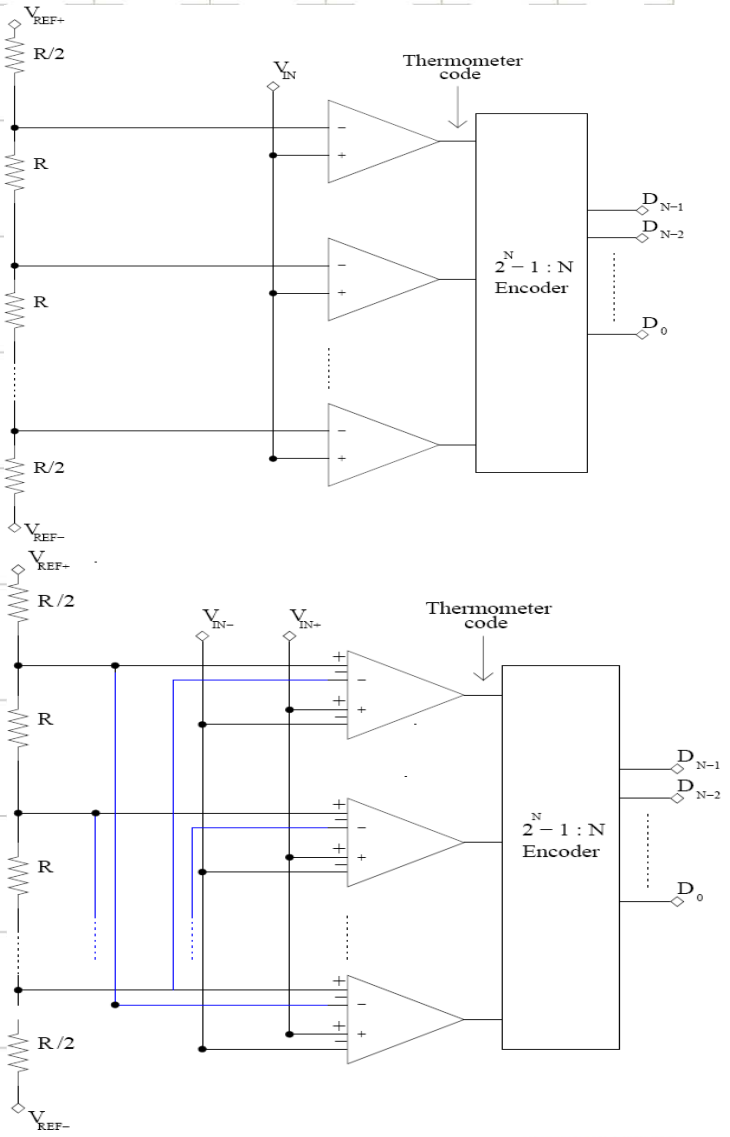
Flash ADC

- Fastest ADC structure
- 2^N resistors , 2^N-1 comparators, thermometer-code to binary encoder
- Single-ended or differential type (wider intensity range)
- Drawbacks (bit wise increase):
  - Area and power double approximately
  - Resistor matching becomes more critical
  - Input bandwidth limited by increasing input capacitance



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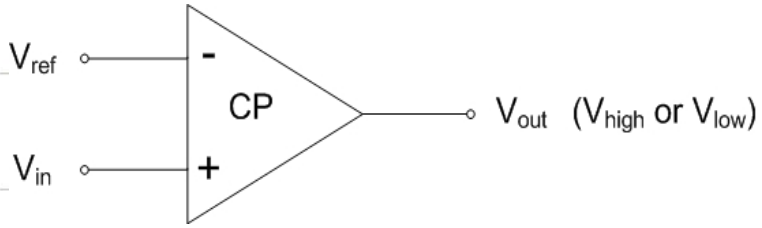
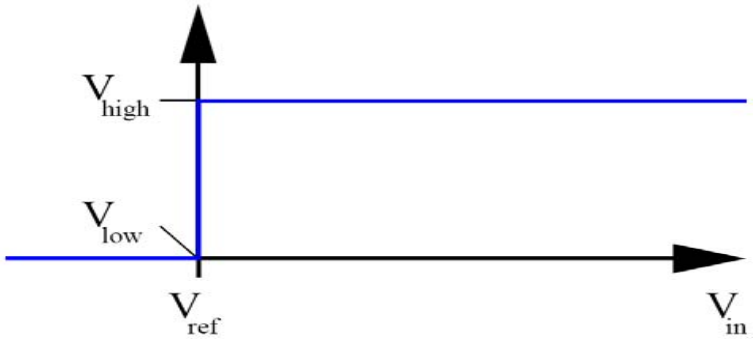
Comparators: Specifications



- Widely used components, especially in ADCs
- Comparator as 1-bit ADC
- Important specifications for implementation in flash ADCs:
  - Bit resolution (≈ maximum bit resolution of flash ADC)
  - Input common mode range (ICMR) (≈ maximum flash ADC approximation range)
  - Speed (≈ maximum speed of flash ADC)
  - Power (≈ minimum power dissipation of flash ADC (after division by the number of comparators))
- No Sample & Hold block needed when clocked comparators are implemented e.g.
  - Latch-type comparators
  - SC-type comparators



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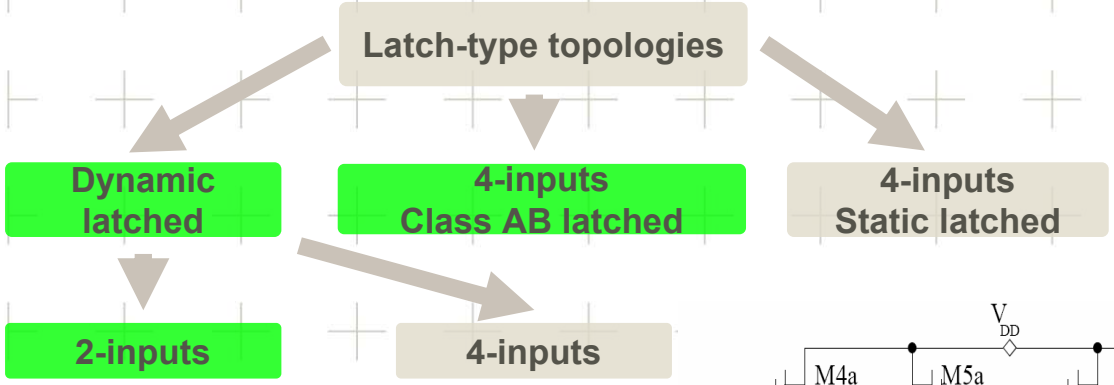
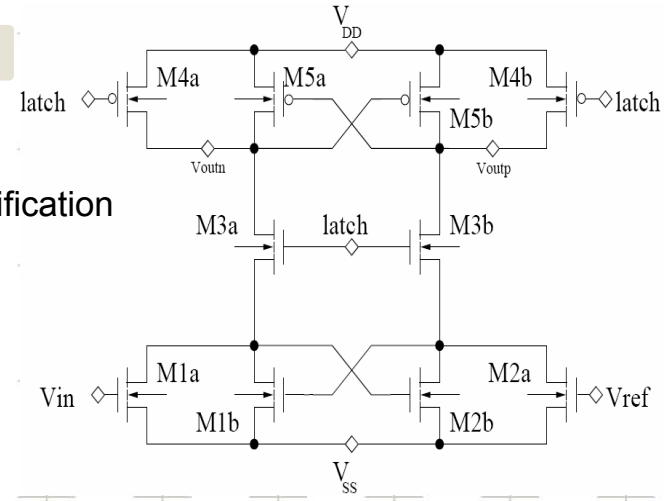
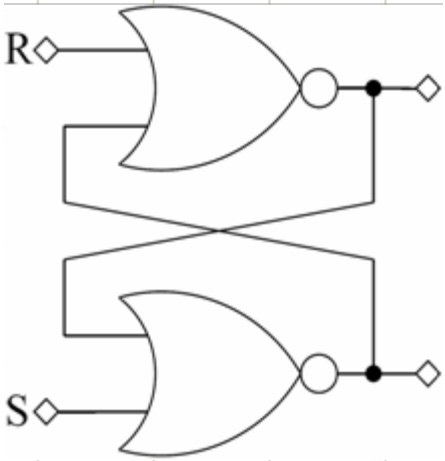
  - Comparator Specifications
  - **Latch-Type Topologies**
  - SC-Type Topologies
  - Simulation Results in 65 nm Technology
- Comparator Selection Procedure
- Flash ADC Testbed Verification in 65 nm Technology
- Conclusion

Comparators: Latch-Type Topologies

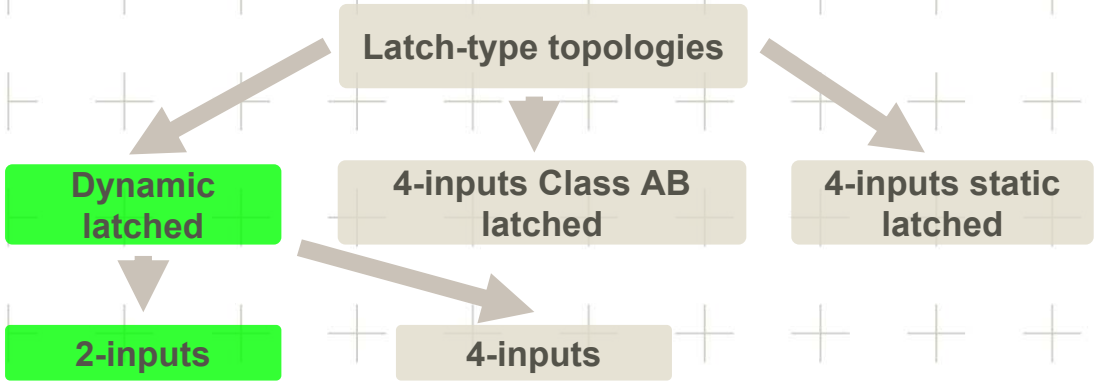


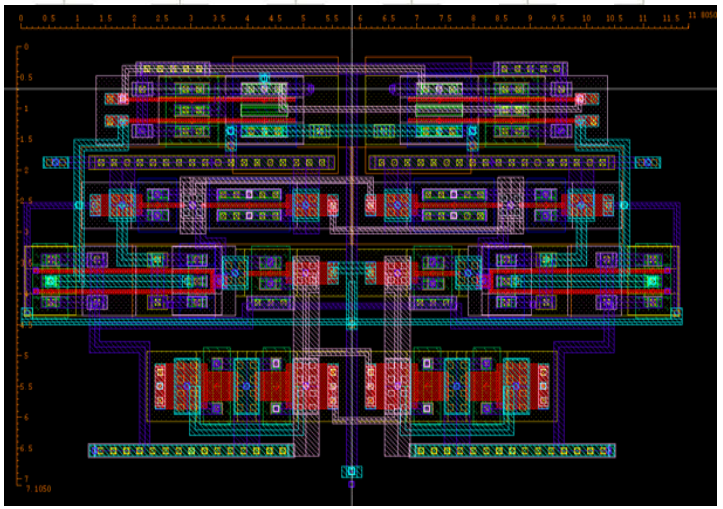




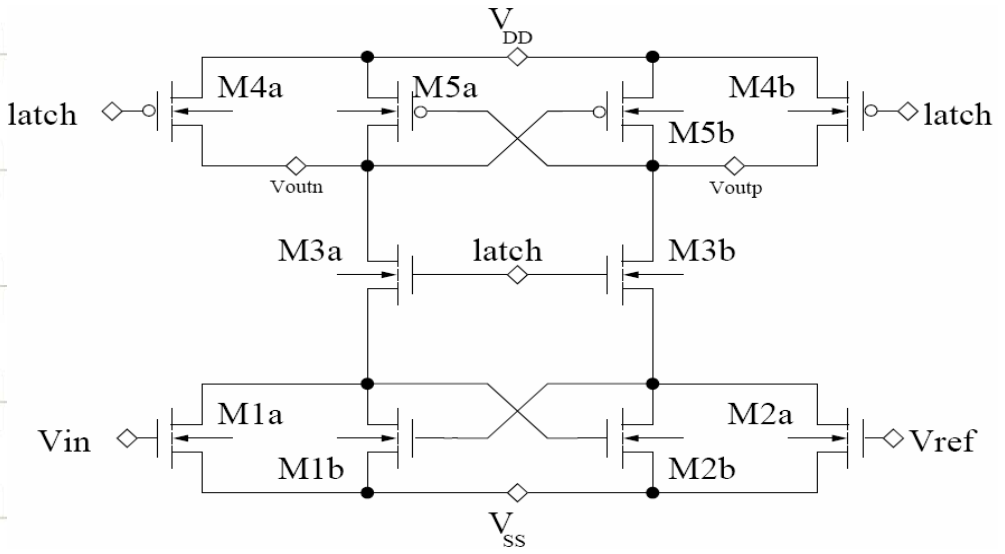
- Principle: Positive-feedback circuit
- Phases: regeneration (latch=0) and amplification
- Advantages:
  - High and rapid amplification
  - Low area
  - Low power
- Disadvantages:
  - Kickback noise is the main challenge (Charge transfer between the input and the positive-feedback circuit when the amplification phase is active)
  - Mismatch and parasitic sensitivity are additional drawbacks
  - Output changes to opposed digital state in the regeneration phase
    - Solution: SR-Latch at the output

Comparators: Latch-Type: 2-inputs Dynamic Latched

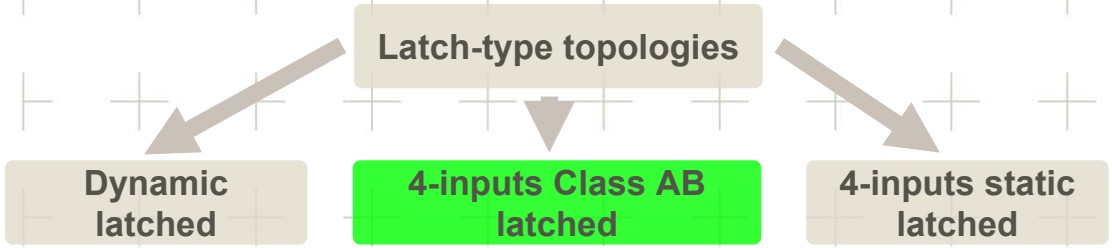


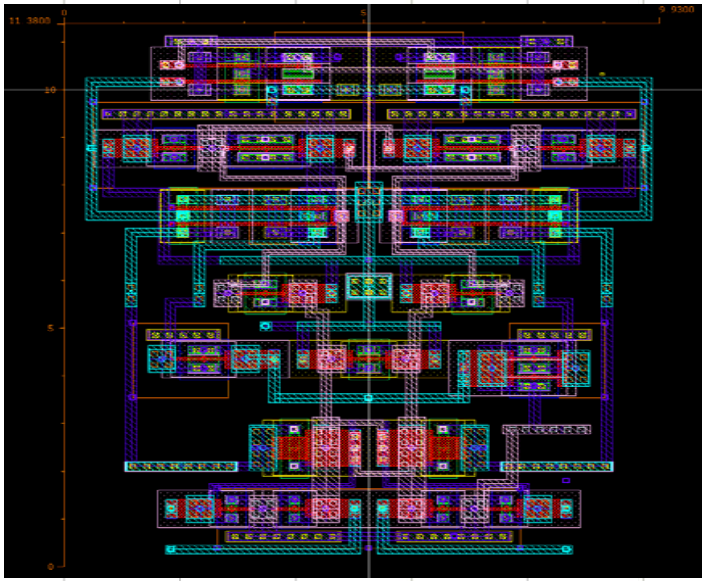


+ High speed
+ Low power
+ Low area
– High parasitic sensitivity
– Limited ICMR

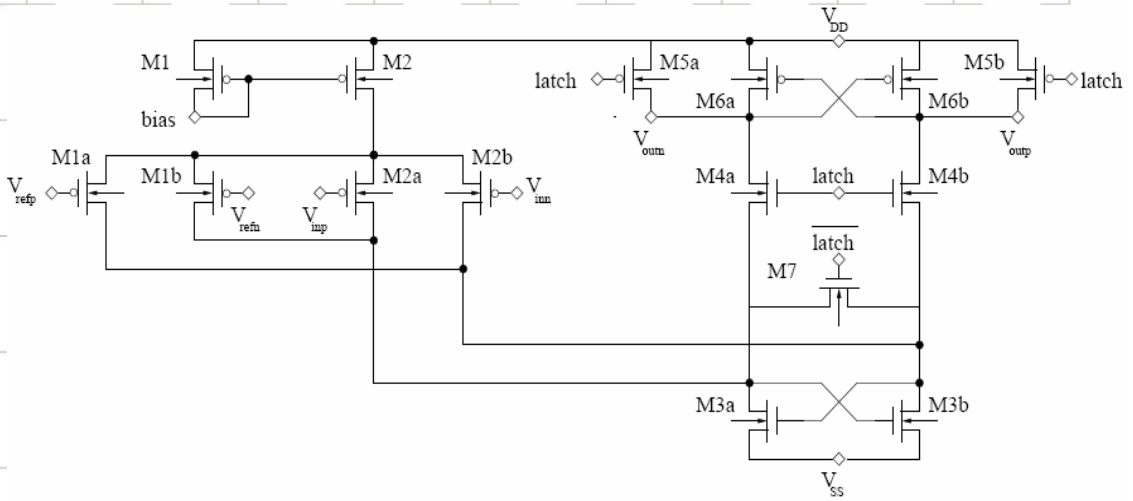


Comparators: Latch-Type: 4-inputs Class AB Latched





+ High speed
+ Low power
+ Low area
+ Rail-to-rail ICMR
– Not equal resolution at different references



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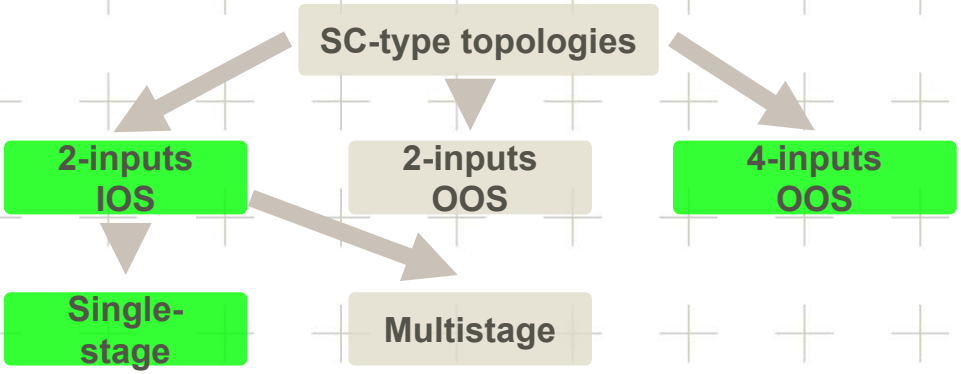
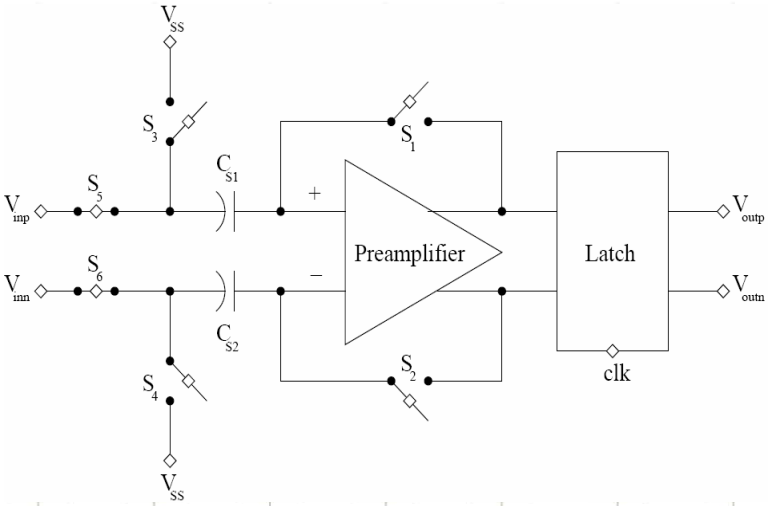
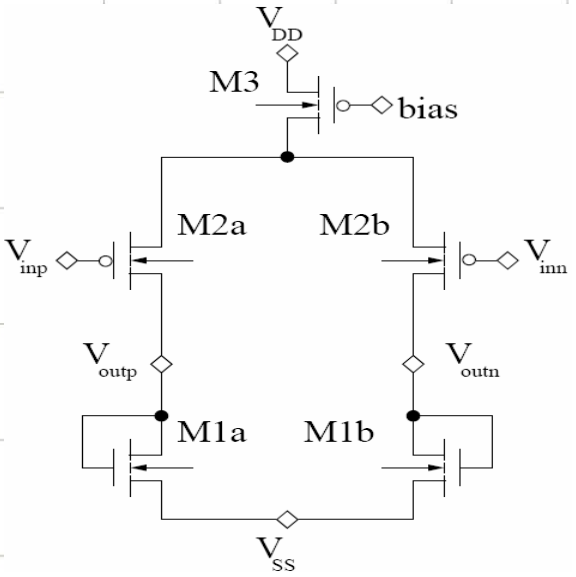
Comparators: SC-Type Topologies

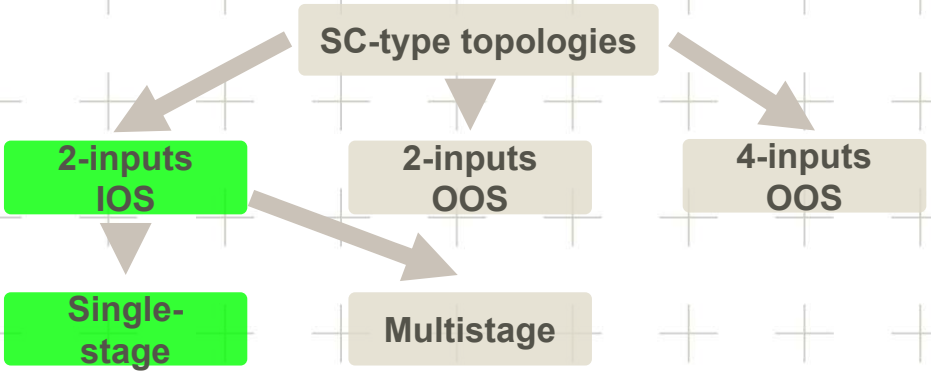


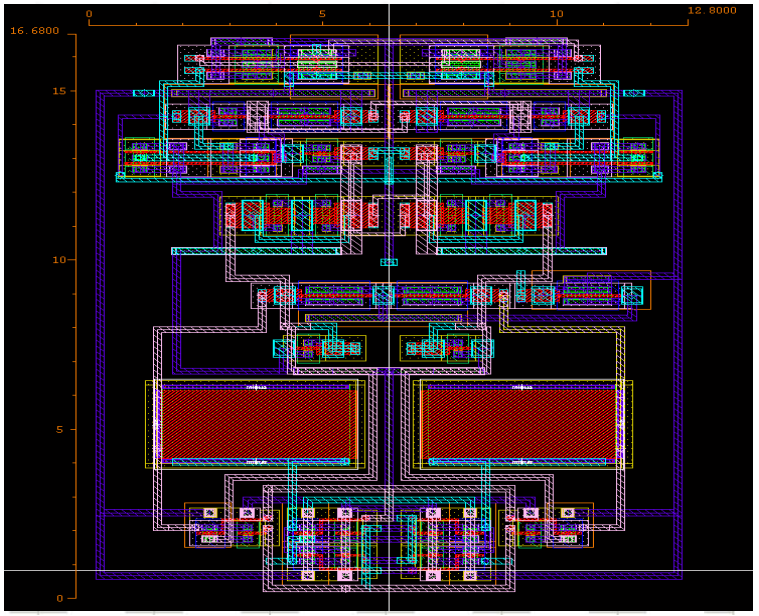


- Principle: Periodically sense and store the offset on capacitors
- Phases: Offset cancellation, amplification and latch
- A PMOS-input differential amplifier is used as the preamplifier
- The latch part is represented by the 2-inputs dynamic latched comparator
- Advantages
  - High Resolution
- Disadvantages
  - High area
  - High power



Comparators: SC-Type: 2-inputs IOS





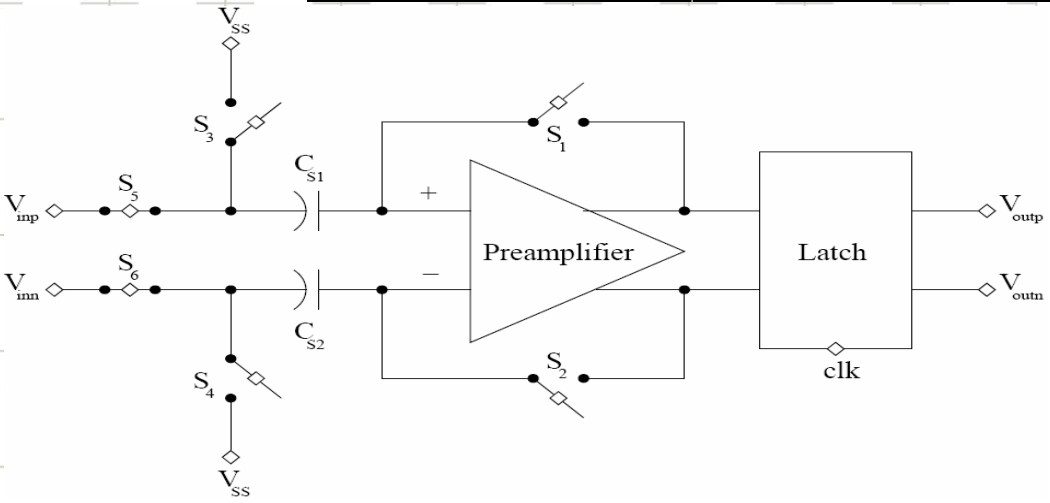
- IOS: Input offset storage

\+ Rail-to-rail ICMR

\+ High resolution

– High area

– High power



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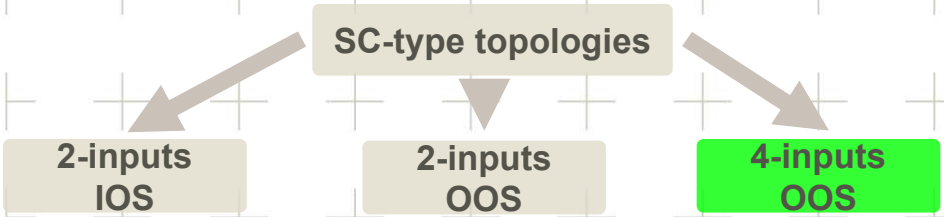
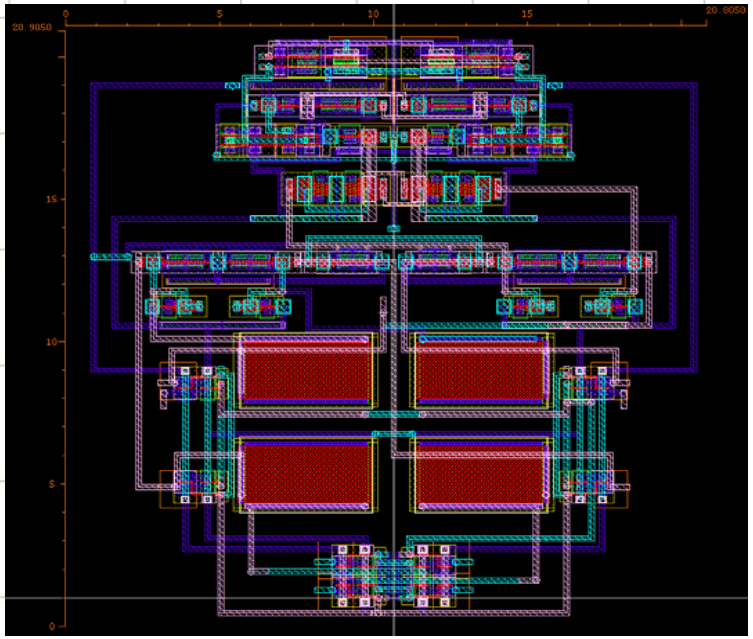
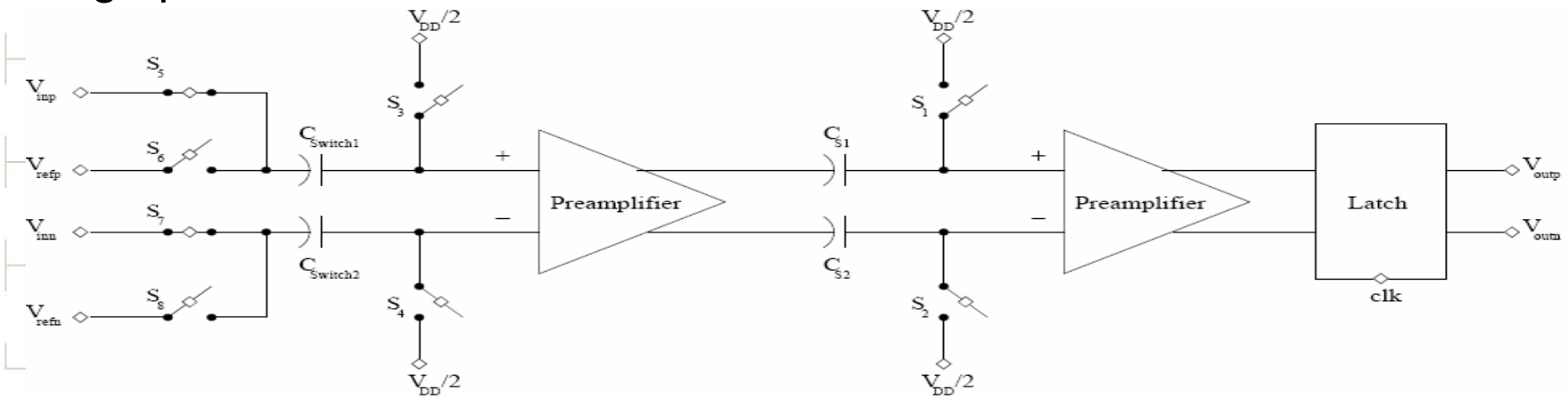
Comparators: SC-Type: 4-inputs OOS





- OOS: Output offset storage

+ Rail-to-rail ICMR
+ High resolution
– High area
– High power



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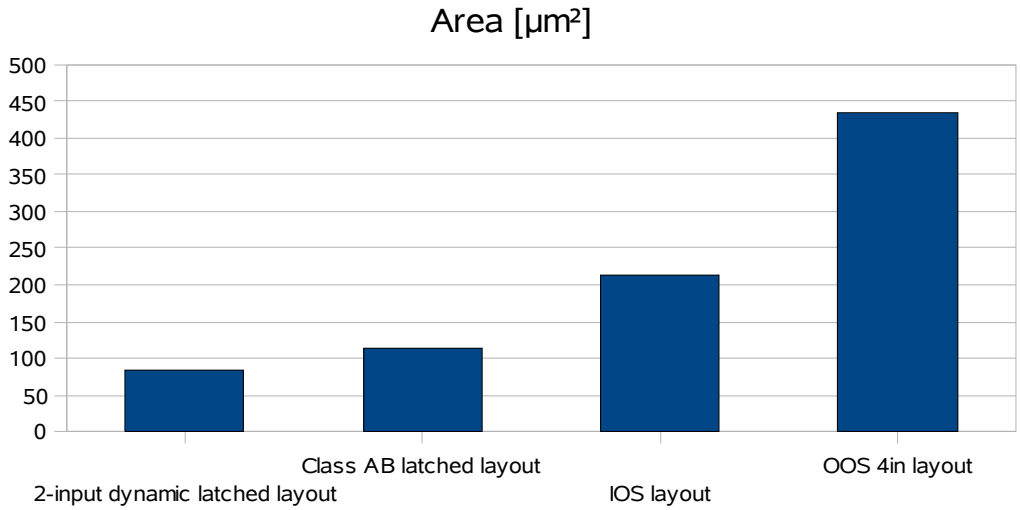
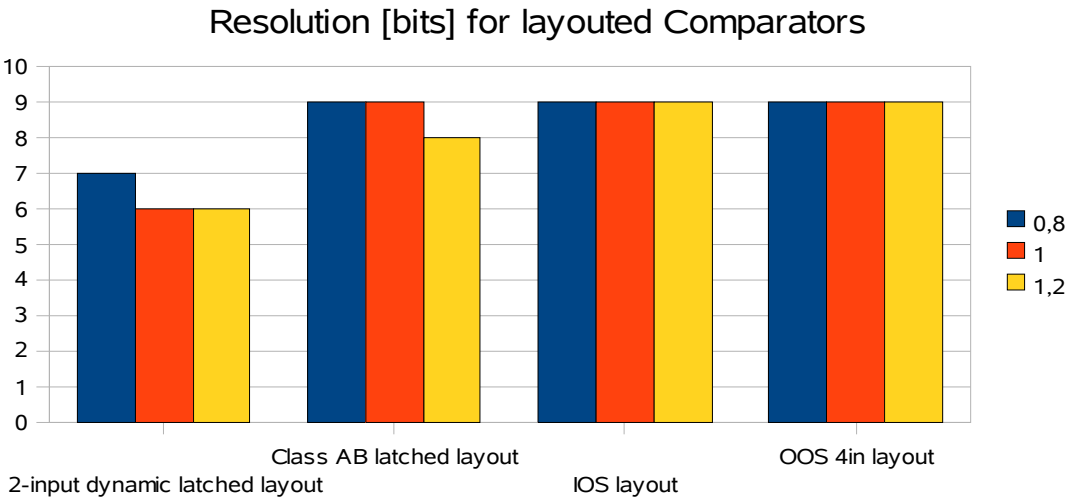
Comparators: Results: Area and Resolution

- Latch-type comparators
  - Low area
  - Parasitic sensitivity degrades maximum resolution
- SC-type comparators
  - High area
  - Less parasitic sensitivity
- Conclusion:
  - Lower area leads to less area consumption





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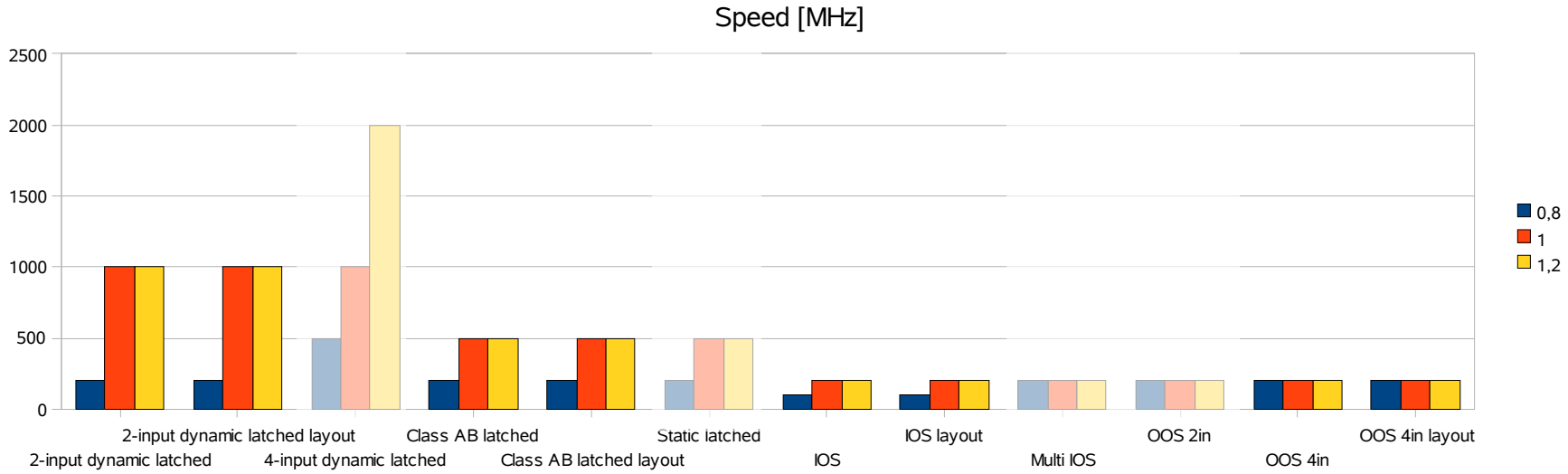
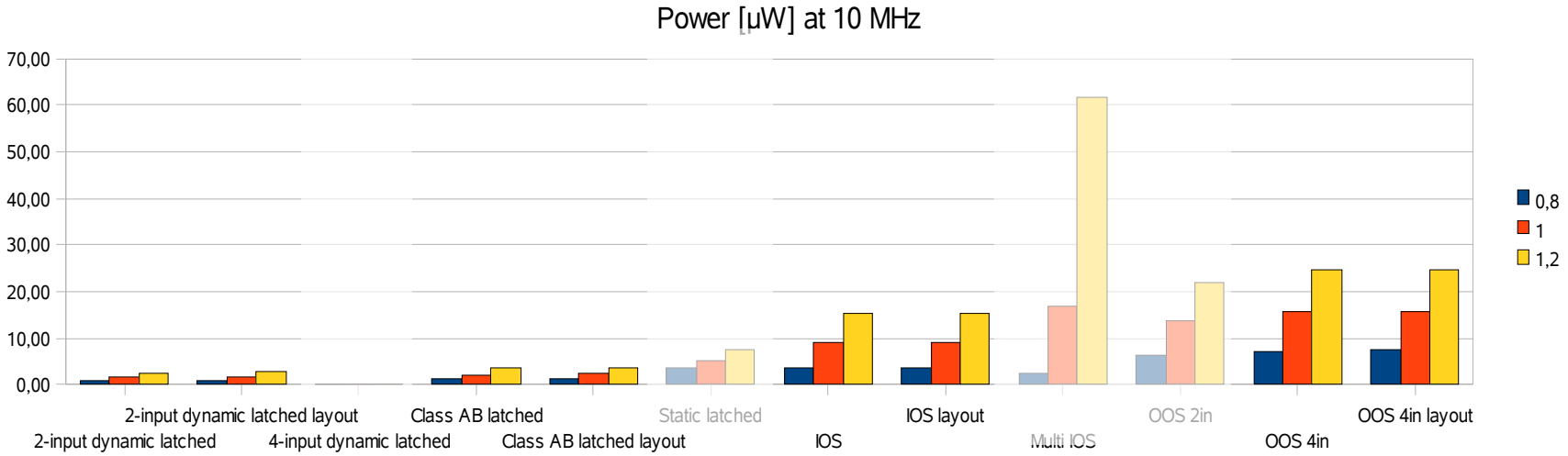
Comparators: Results: Speed and Power





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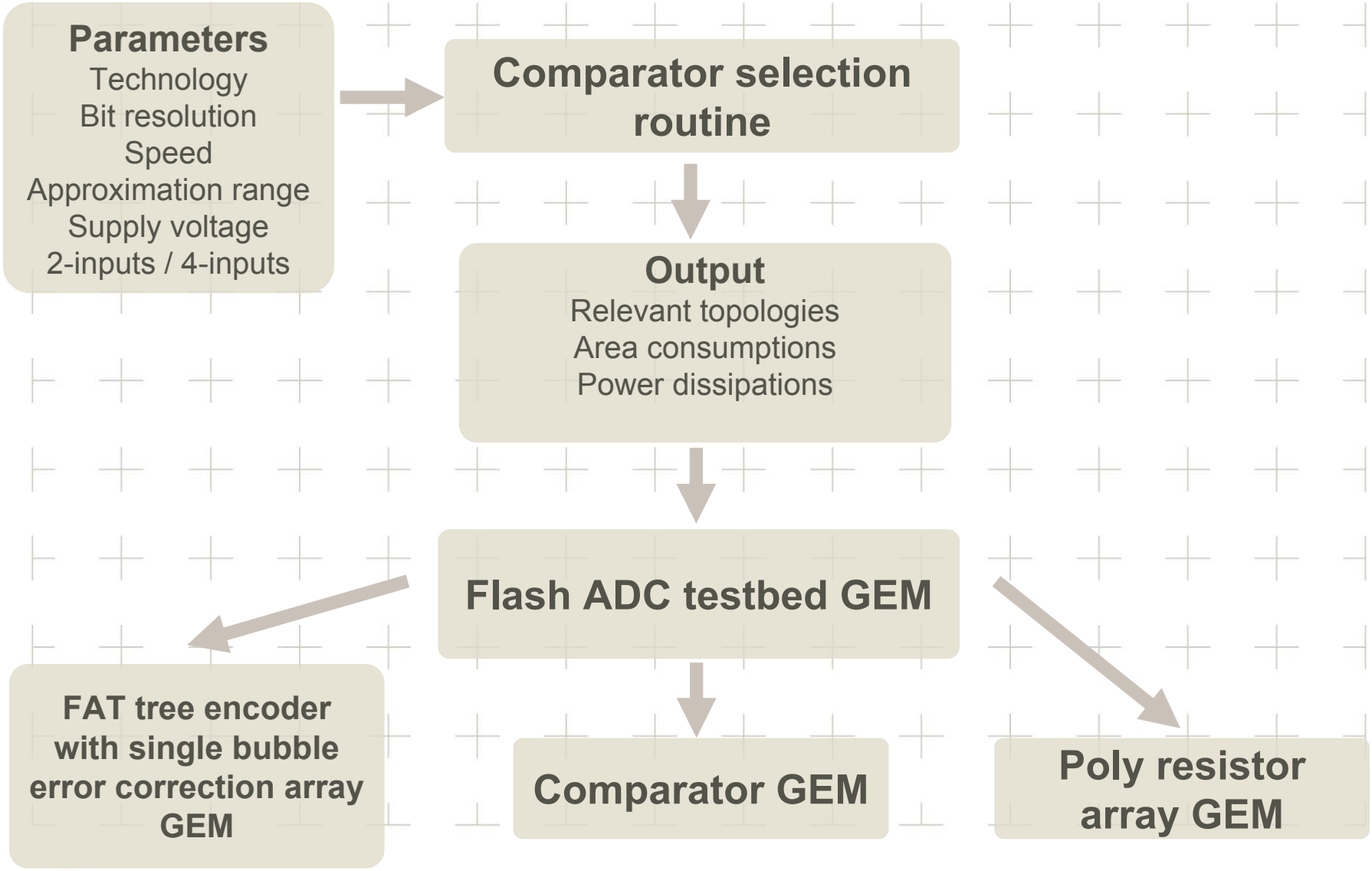
Comparator Selection Procedure



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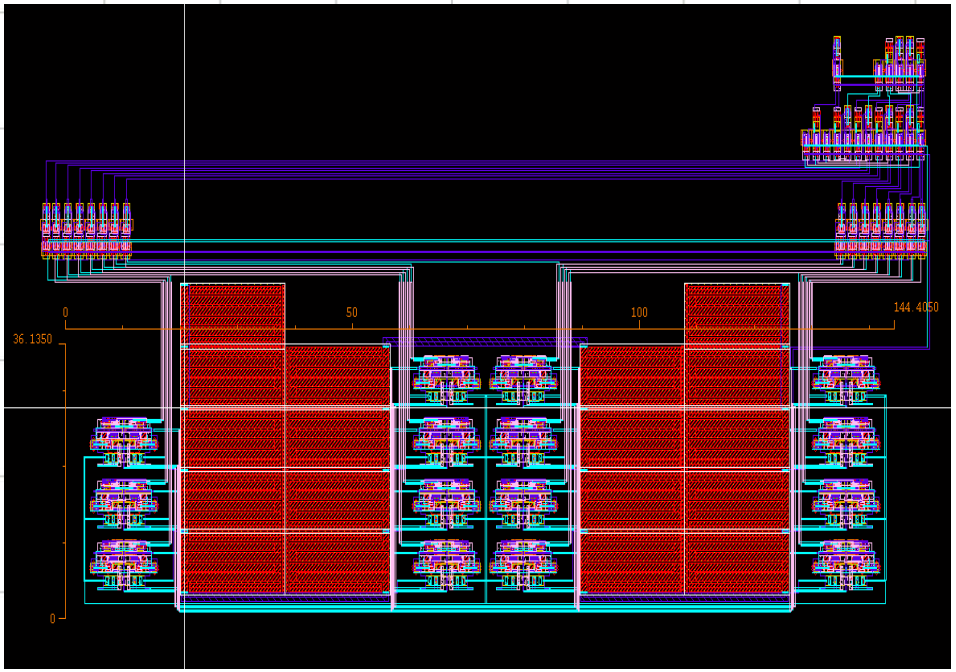
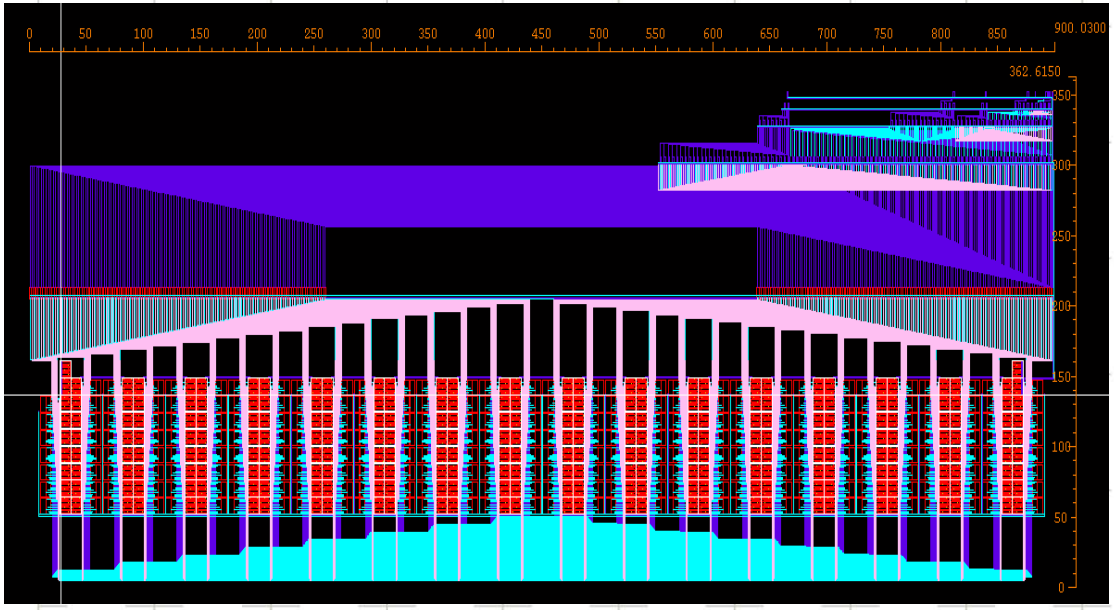
Flash ADC Testbed: Layouts: 4bit-flash ADC

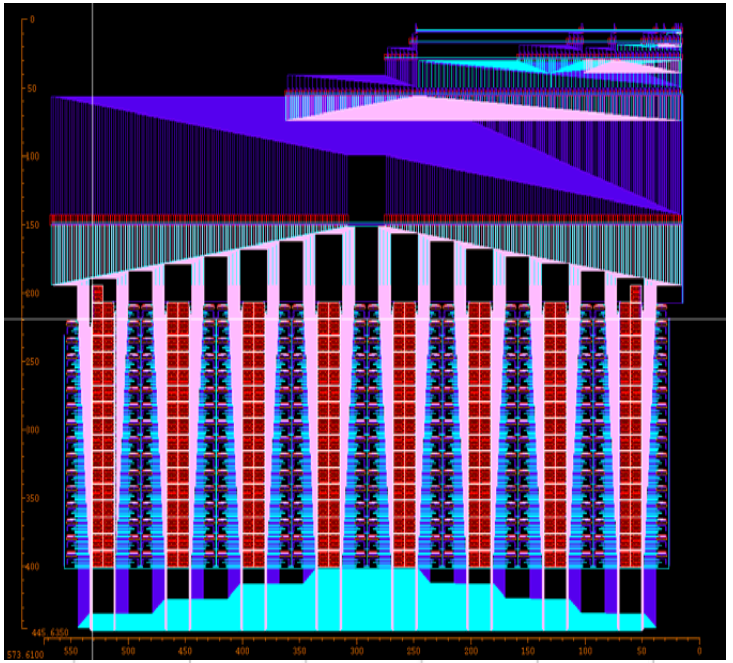
- Checked and verified for resolutions between 4 and 10 bit (DRC & LVS)
- Compatible for all analyzed comparators
- Dimension scalability:
  (x-y distribution of comparators & resistors is adjustable)



4bit Flash ADC layout; Implemented comparator: 2-inputs dynamic latched

Flash ADC Testbed: Layouts: Dimension Scalability with 8bit-Flash ADC





- Scalable X-Y distribution of resistors & comparators
- Left: 32 blocks with each 8 comparators & resistors
- Right: 16 blocks with each 16 comparators & resistors
- Implemented Comparator: 4-inputs Class AB latched

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  - **DNL/INL Results**
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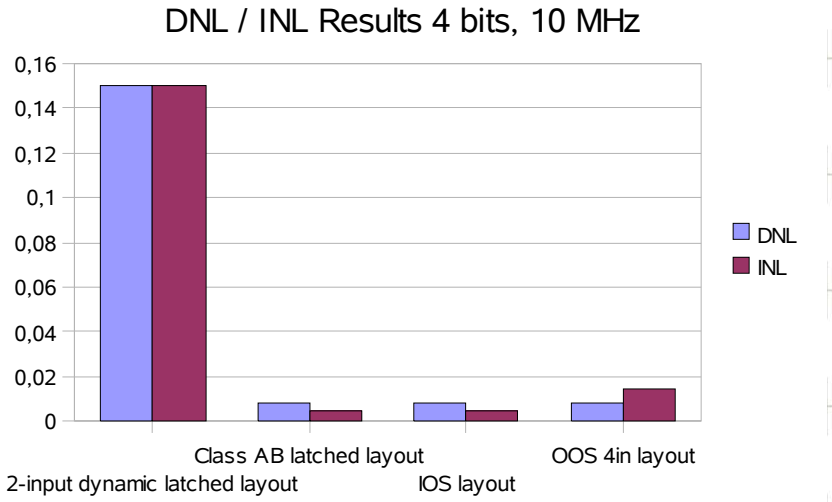
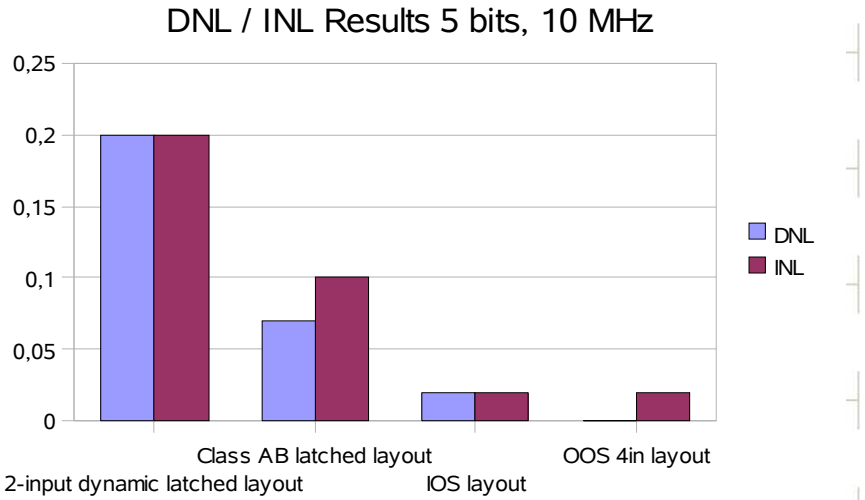
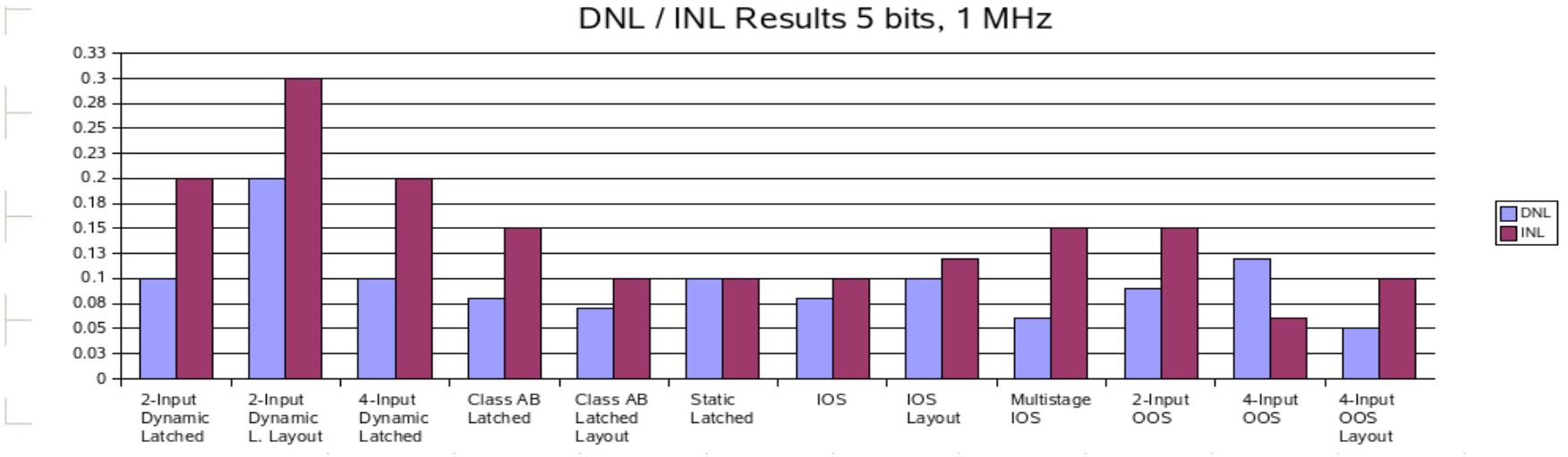
Flash ADC Testbed: DNL / INL Results







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Conclusion

- Investigation of relevant comparator topologies:
  - Latch-type comparators:+ high speed, + low area, + low power, - high parasitic sensitivity
  - SC-type comparators: - low speed, - high area, - high power, + low parasitic sensitivity
- Investigation and implementation of comparator selection procedure for the flash ADC testbed
- A flash ADC GEM testbed has been developed, which is compatible to all analyzed comparators
  - Checked and verified (DRC, LVS) for resolutions between 4 and 10 bits
  - Integration of x-y dimension scalability
  - Complex FAT tree encoder with single bubble error correction array implemented
  - Functional verification (simulation of schematic and extracted layout view) has been done in 65 nm technology
  - Selection methodology verified for all analyzed comparators
- Main advantage of the selection methodology:
  - Simplification of selection and implementation of flash ADCs referring to high-level demands

Thank you for your attention!