# Development of a 24GHz fully integrated VCO

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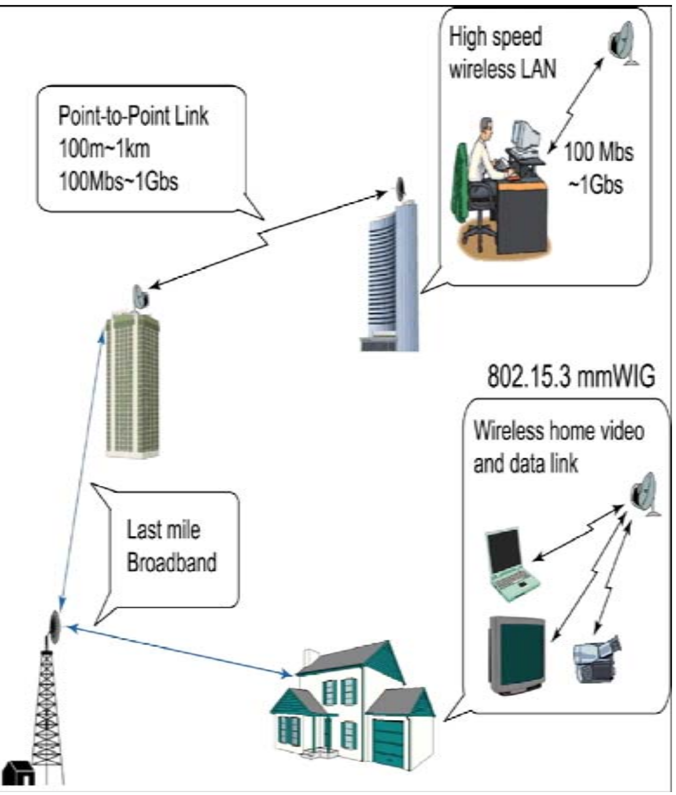
IMST

# Wireless Communication




## Cellular Telephones

## wireless LAN's

## GPS/satellite

## Receivers

small size

low power

low-cost

small form

# Voltage Controlled Oscillators

- **Applications**
  - *PLL-Based Applications*
  - *Non-PLL Based Applications*

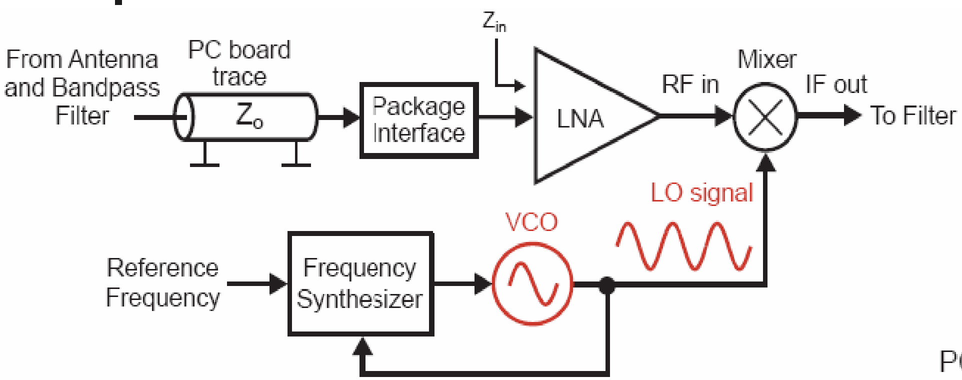
# Voltage Controlled Oscillators

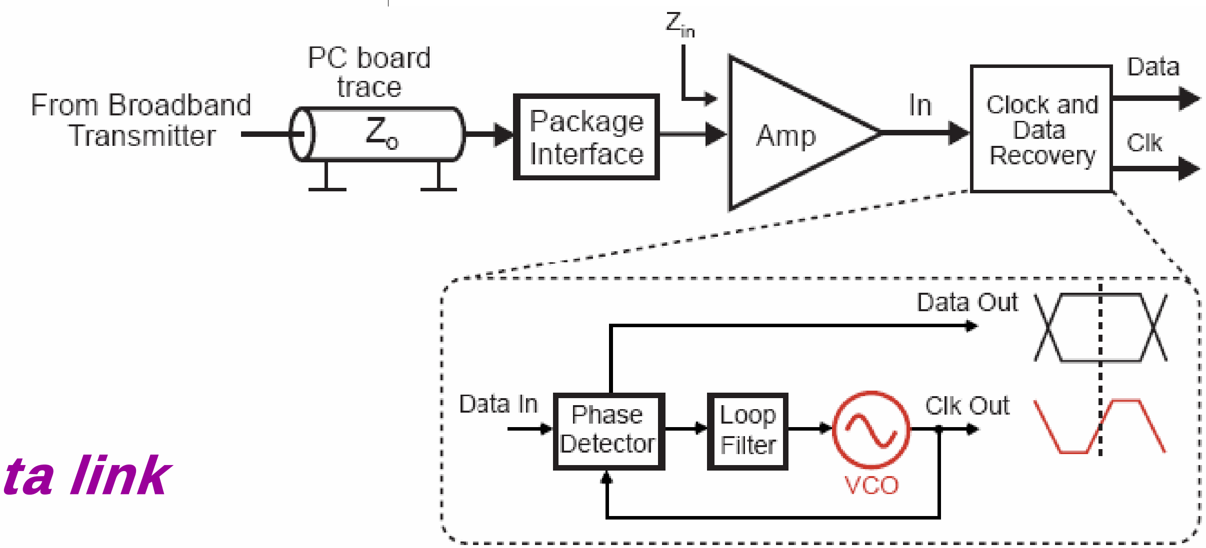
- **Applications**

*Base Station*
*Cell Phone*
*Telecommunication*
*GPS & Navigation*
*Satellite Communication*
*LAN/WAN*
*Military*

# VCO in Digital & Analog Applications

*VCO for Analog wirless system*




*VCO for High speed data link*

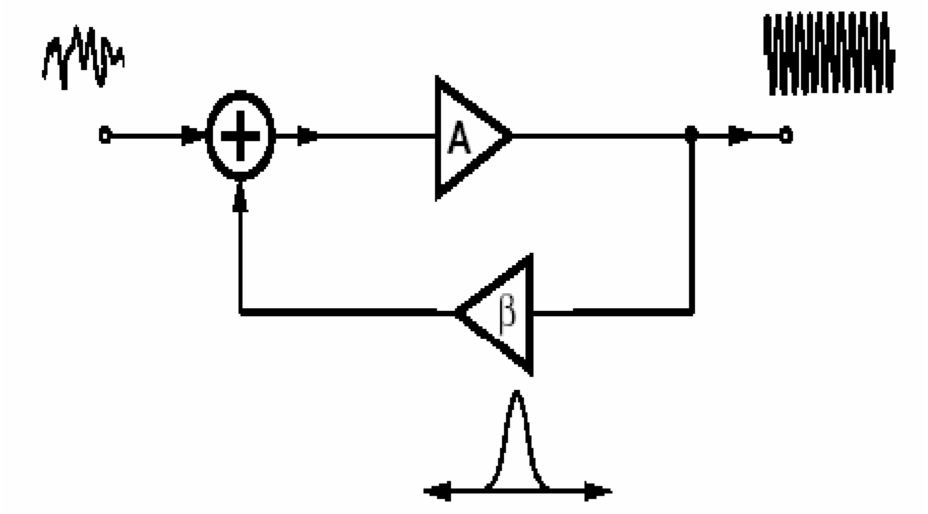
# Design Goals

- Design integrated on-chip inductor optimized for low phase noise
- VCO Core
- Stable on-chip  power amplifier
- The matching between the core and PA and PA and load

# Target Design Specifications

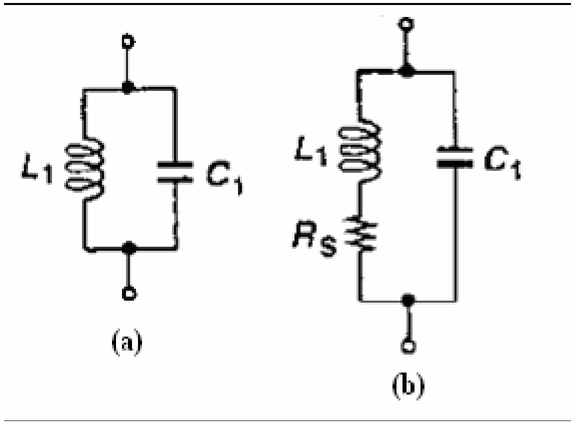
- Frequency 23.9- 24.35 GHz
- Out put Power 6 dBm
- Supply Voltage 3.2V to 3.4V
- Supply Current <50mA
- Phase Noise <-70 dBc/Hz @ 100 KHz offset
- Tuning Voltage Range 0.4 to 2.8 V
- Temperature Range -40° C to 105° C
- Layout < $1\,mm^2$

# Some Theories




$$H(s)=\frac{A(s)}{1-A(s)\times\beta(s)}$$

# Some Theories




$$\frac{-1}{j\omega c_1}$$

$$f = \frac{1}{2\pi\sqrt{LC}}$$

$$j\omega L_1$$

$$Q \rightarrow \infty$$

# How about the VCO?

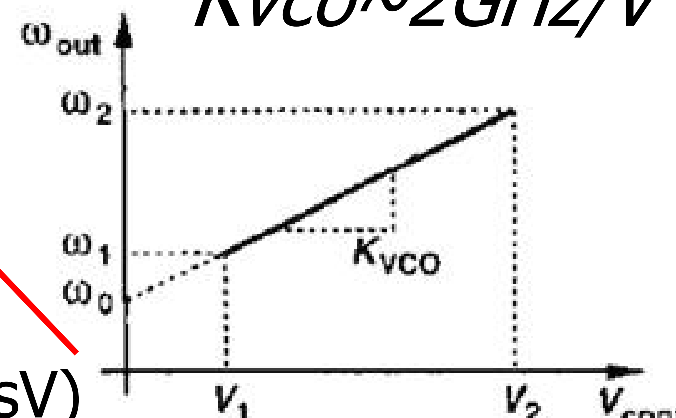

L~70 pH

C~0.65pF

f~24 GHz

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont}$$

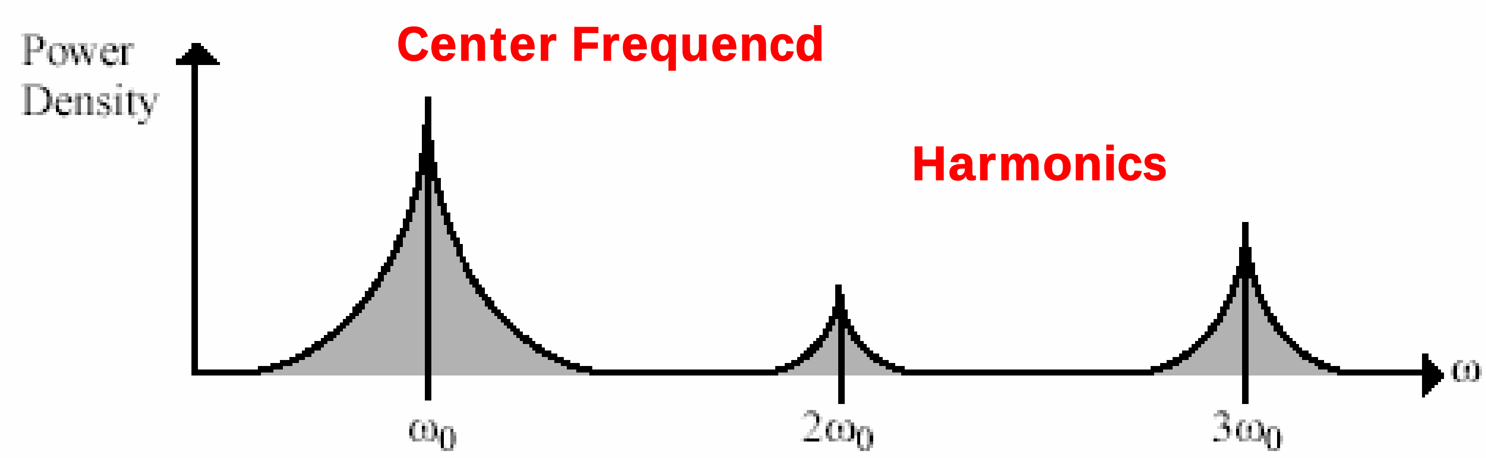
*Kvco~2GHz/V*




*Vcont= 0*

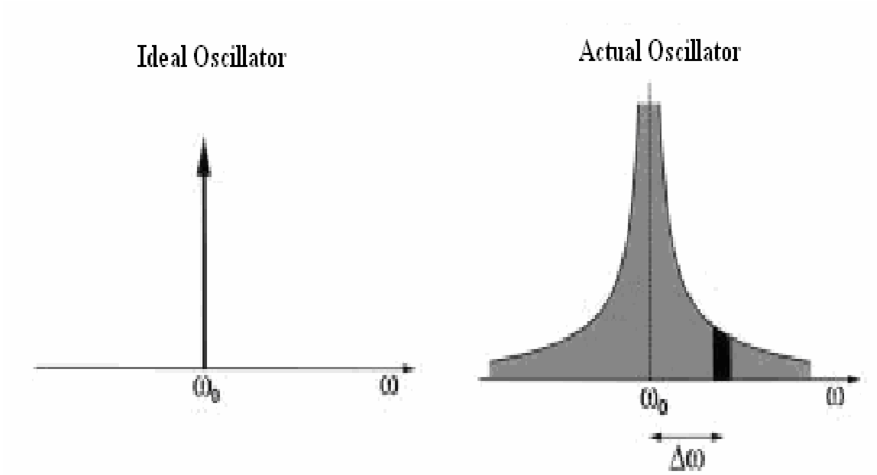
VCO gain (rad/sV)

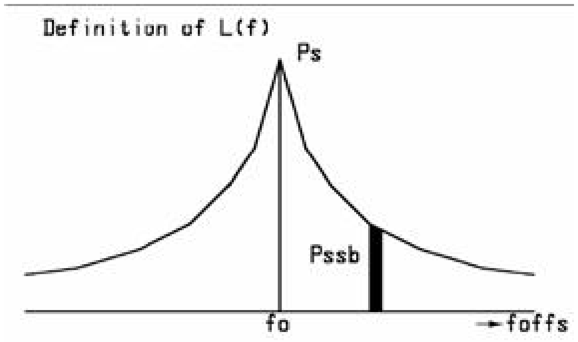
# Noise in Oscillators




**Practical Oscillator Spectrum**

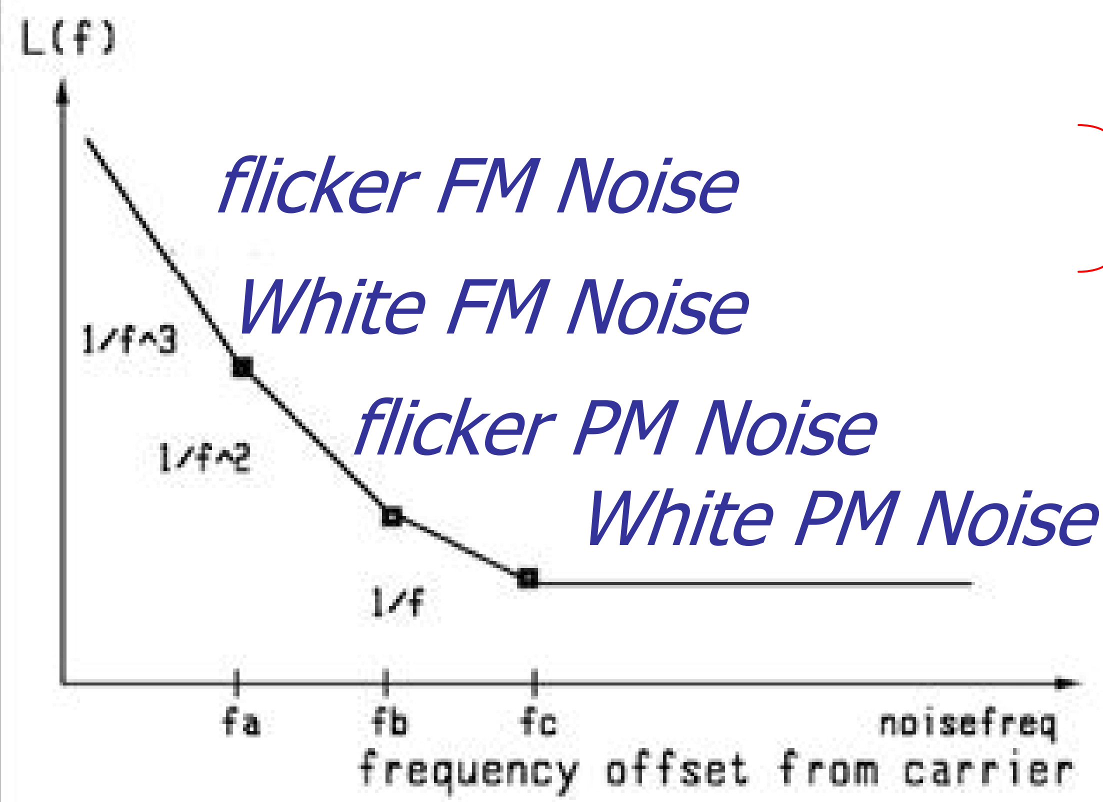
# Phase Noise




$$L(f)=\frac{P_{ssb}(per\,1Hz)}{p_s}$$

# Phase Noise




**frequency modulation**

**mixes up to the oscillation frequency**

# Leeson's Model

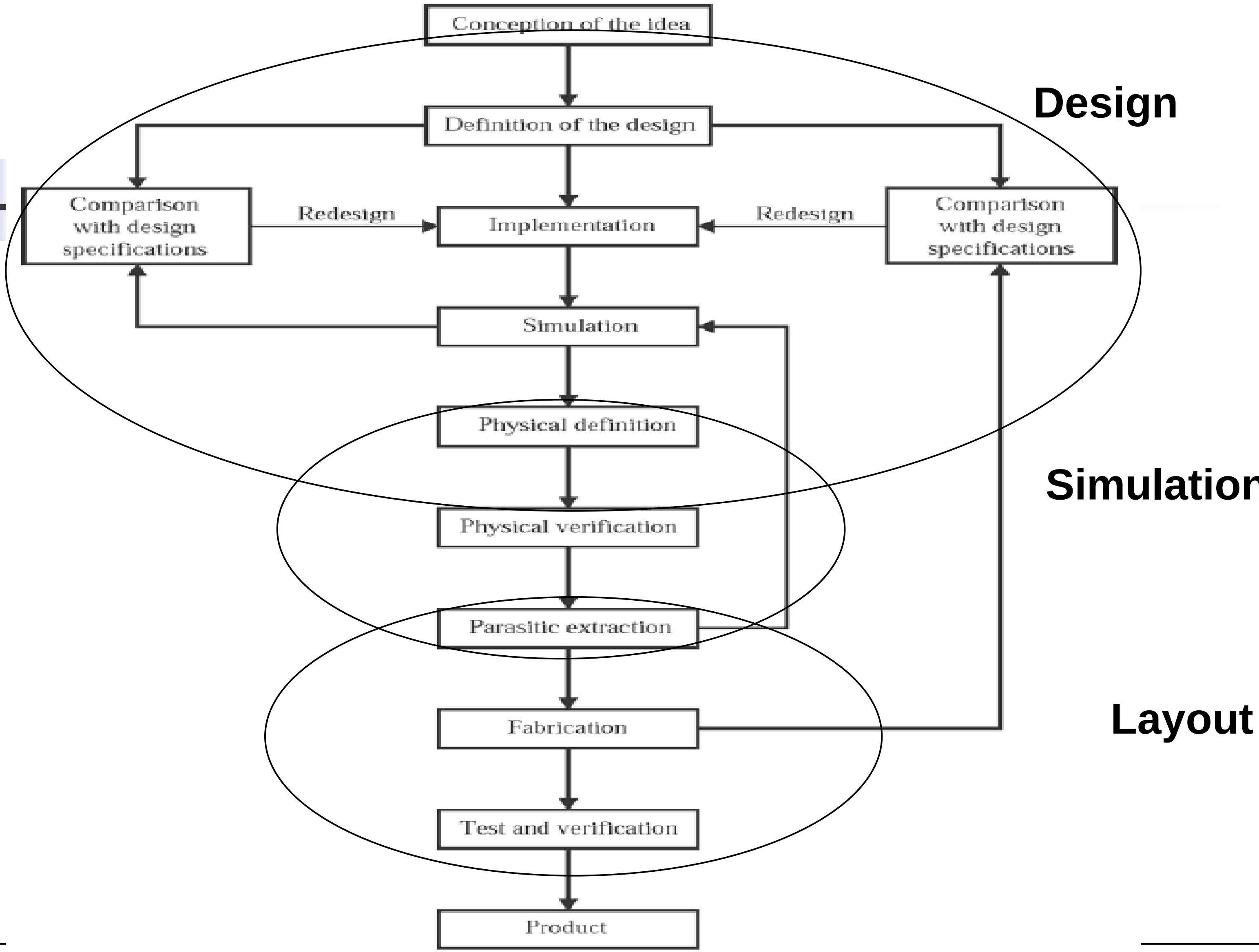
$$L\{\Delta\omega\}=\left\{\frac{2FKT}{P_S}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left[1+\frac{\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right]\right\}$$

- *Q* is the quality factor of the tank
- *Ps* is the average power dissipated in the tank

# How to reduce Phase Noise

- The average power dissipated in the tank resistance
- Quality factor with the Power 2
- Low Noise Power Supply and Tuning Voltage
- Grounding HF and DC
- Connections to the tuning port: short, screened, shielded, decoupled
- Capacitor Bank

# Design Process flow for Analog Integrated Circuits



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# The applied technology

- **B7HF200_8 200 GHz Bipolar technology**

**200 GHz SiGe / ( silicon-germanium) bipolar process with copper metallization for mixed analogue / digital HF applications**

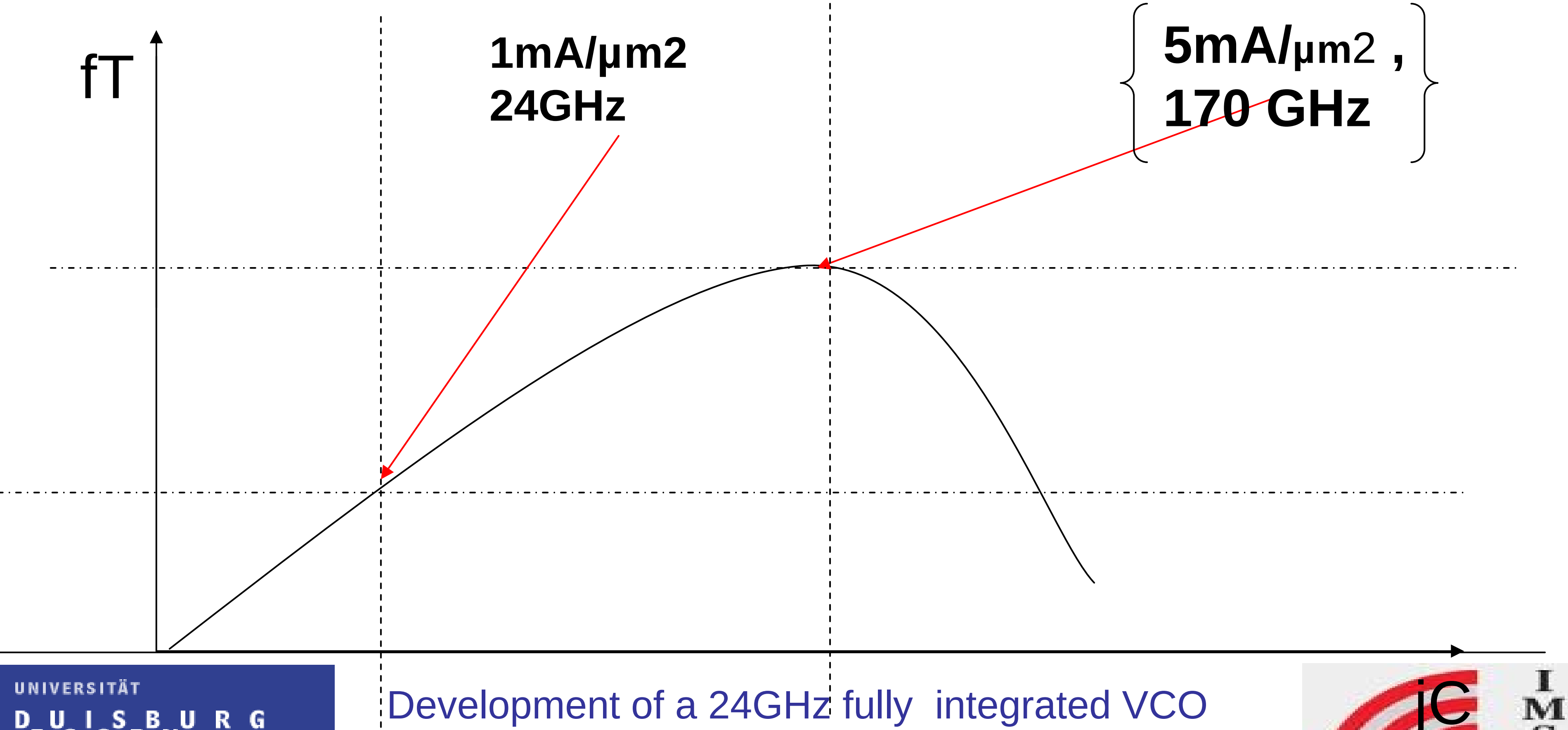
High speed and ultra high speed npn Transistors

Varactors MIM capacitors 3 kind of Resistors

**No Inductor**

# Frequency Operation Point

fT (@ jC = 5 mA/µm2) = 170 GHz , $V_{(BR)}$=1.5-6



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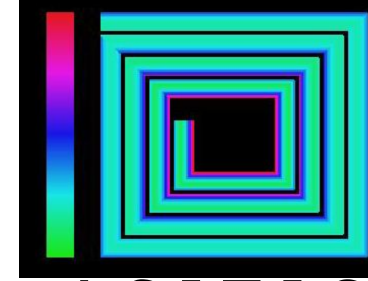

ASITIC

# *Inductors*

On-chip spiral inductors

Very non ideal behaviour

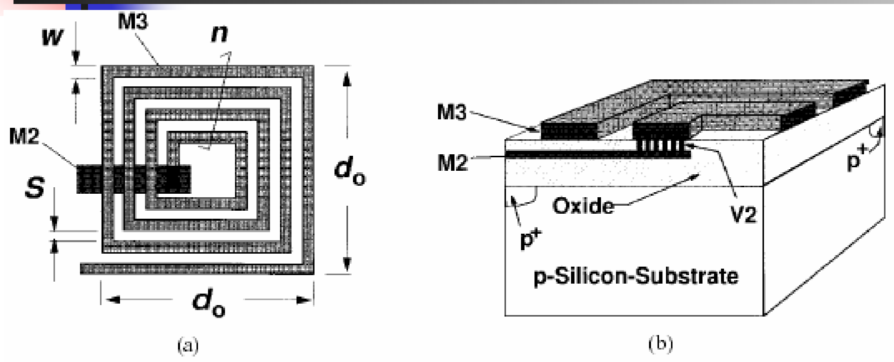
Rather low Q

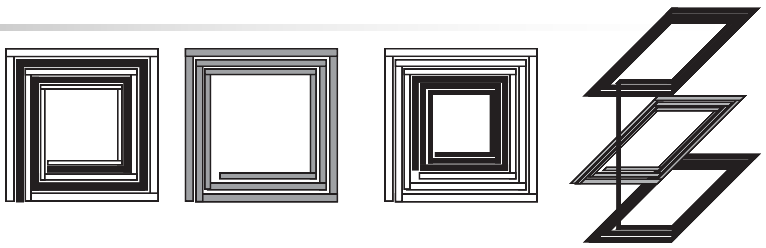
Size depends on the current

Width< 15 um

Symmetric, Differential L=70pH Q=15

# Losses in Integrated Inductors



metal & via resistance constant

low frequencies,

Q proportional to Frequency and affected bye the substrate.

higher frequencies

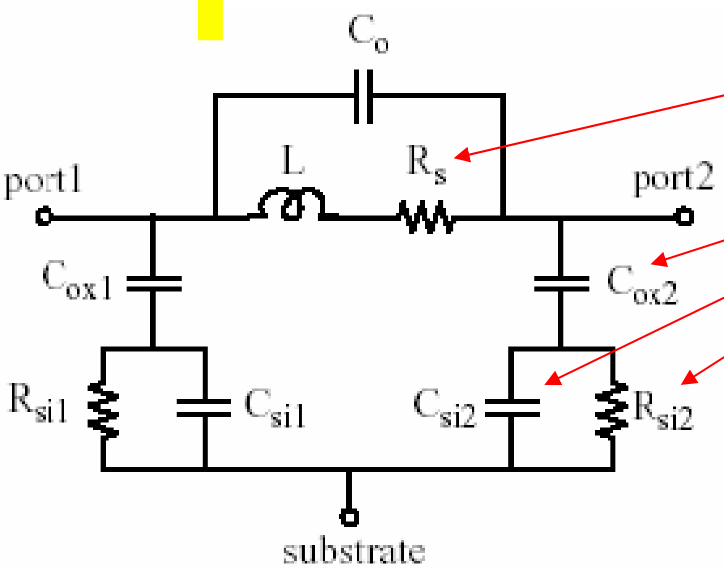
Q directly proportional to frequency skin effect

Q is proportional to square root of Frequency.

# Greenhouse's Model

Series resistance of the spiral

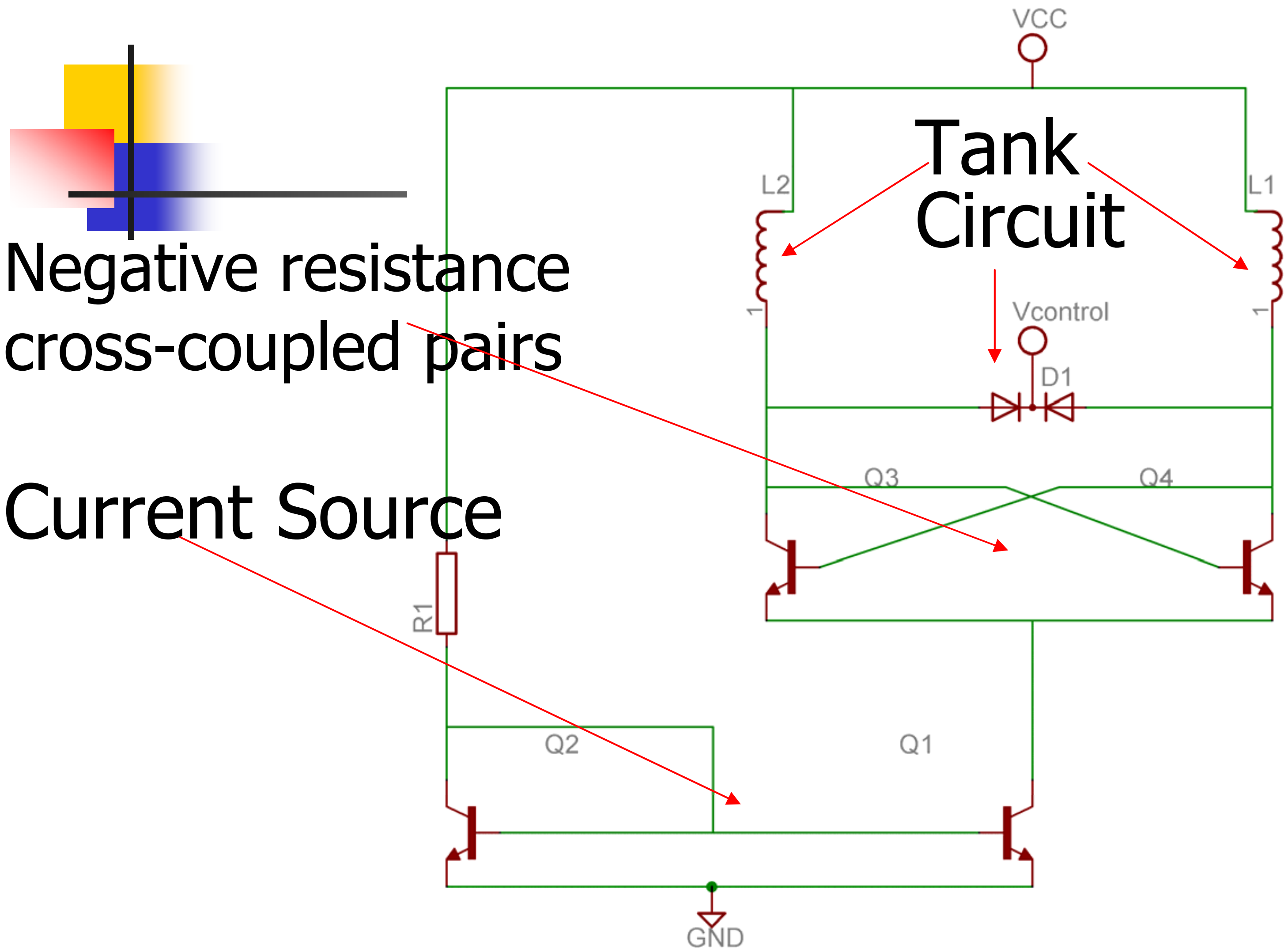
between the metal layer and subtrate




What affects the resistance of a microstrip line in a silicon technology?

DC Current, Edge effect, Proximity effect and Skin effect

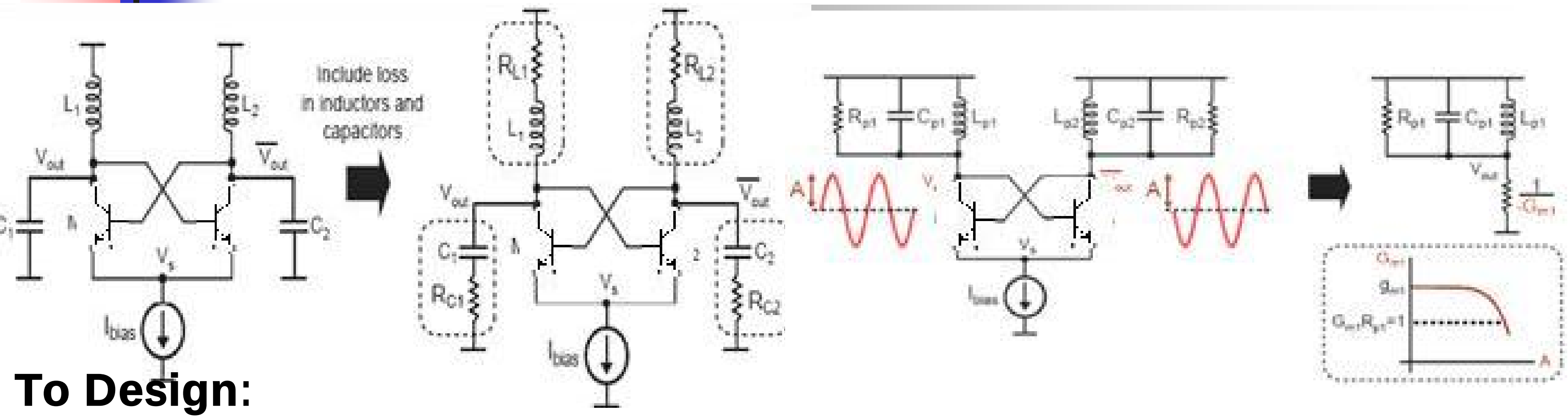
# VCO Core


Tank Circuit
Negative resistance cross-coupled pairs
Current Source
VCC
L2
L1
Vcontrol
D1
Q3
Q4
R1
Q2
Q1
GND

# Negative Resistance Circuit

- **Advantages :**
- Simple topology
- Good for feeding differential circuits
- Good phase noise performance can be achieved, it can reject common mode noise,
- Has better power supply noise rejection,
- Easier to bias on-chip without any ideal ground available.

# Analysis



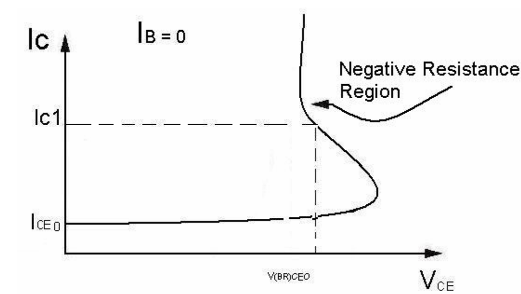

**To Design:**

1.tank components

2.bias current

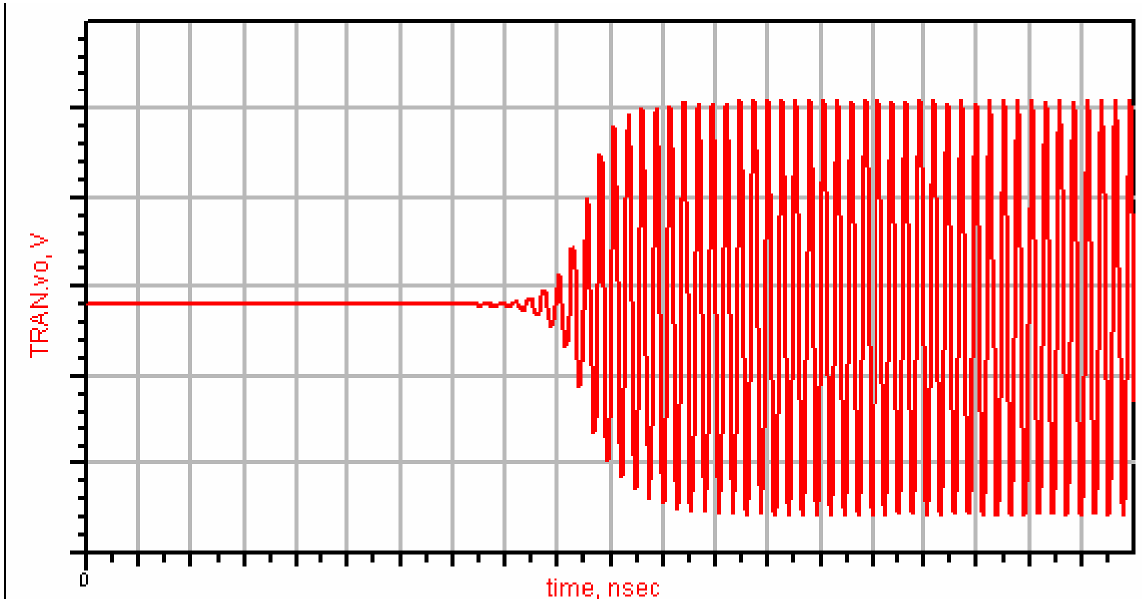
3.transistor size

Gm is the large signal transconductance value




c)collector-Emitter

# Simulation Results




1.8 V p-p

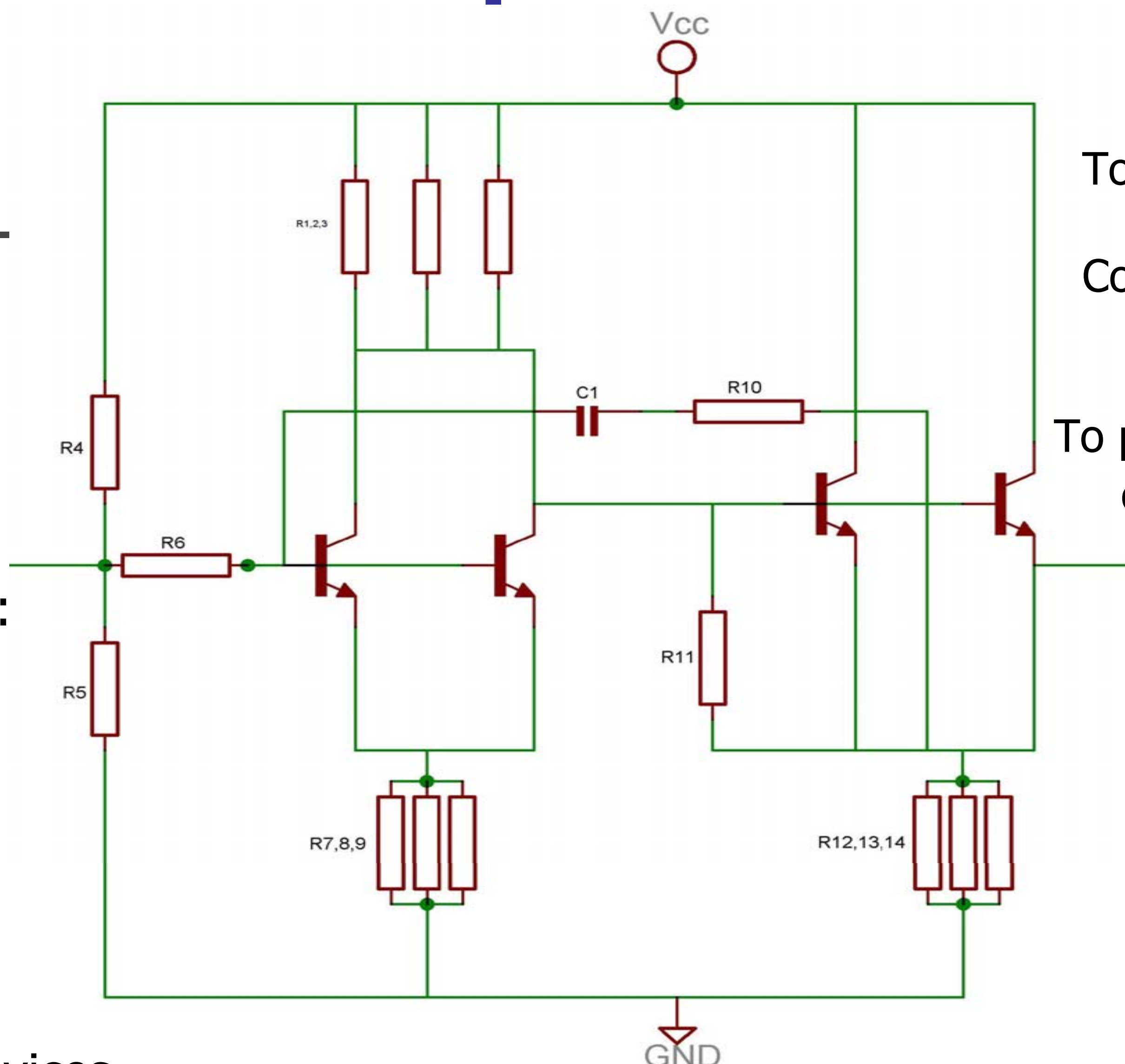
# Amplifier

Biasing
in
Class A

Disadvntage:
Conduction
angel

Battery

Active devices




To decouple the

Core & external load.

To provide sufficient
output power.

# Fourier analysis of the Current wave form

$$I_n = \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\frac{\alpha}{2})}\left[\cos(\theta)-\cos(\frac{\alpha}{2})\right]\cos(n\theta)d\theta$$

$$I_{dc} = \frac{I_{max}}{2\pi}\frac{2\sin(\frac{\alpha}{2})-\alpha\cos(\frac{\alpha}{2})}{1-\cos(\frac{\alpha}{2})}$$

$$P_{dc} = V_{dc} \times I_{dc} \qquad P_1 = \frac{V_{dc}}{\sqrt{2}}\frac{I_1}{\sqrt{2}}$$

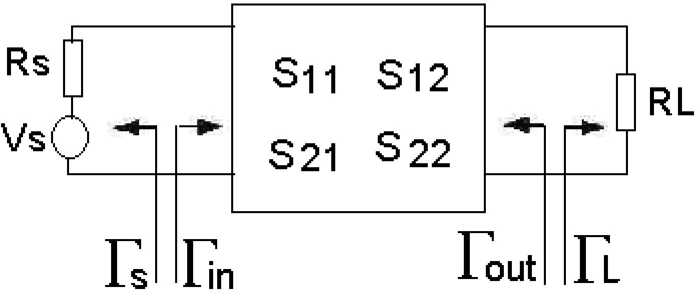
**20Log V = 6dBm , V=0.44**

**Ac denn 0.44*1.4 = 0.63 v Amplitude**

**10Log(P)= 6dBm p=4mW**

**P=R*I^2 I=9mA**

# Stability Calculations




The circuit is Unconditionally Stable if

$$|\Gamma_{in}| \prec 1$$

and

$$|\Gamma_{out}| \prec 1$$

for all values of Rs and RL

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \succ 1 \qquad \Delta = S_{11}S_{22} - S_{12}S_{21}$$

# Stability Circles

- Drawing the locus of the source and load terminations on the Smith Chart

for Source stability Circle $|\Gamma_{out}| = 1$

$$r_s = \frac{|S_{12}S_{21}|}{S_{11}^2 - \Delta^2} \qquad C_s = \frac{(S_{11}\Delta S_{22}^*)^*}{S_{11}^2 - \Delta^2} = |C_s| \measuredangle \theta$$

for Load stability Circle $|\Gamma_{in}| = 1$

$$r_L = \frac{|S_{12}S_{21}|}{S_{22}^2 - \Delta^2} \qquad C_L = \frac{(S_{22}\Delta S_{11}^*)^*}{S_{22}^2 - \Delta^2} = |C_L| \measuredangle \theta$$

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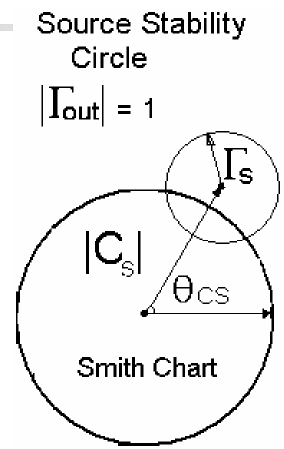
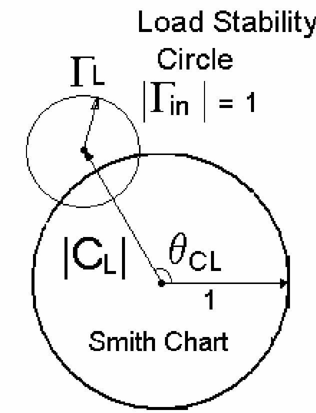
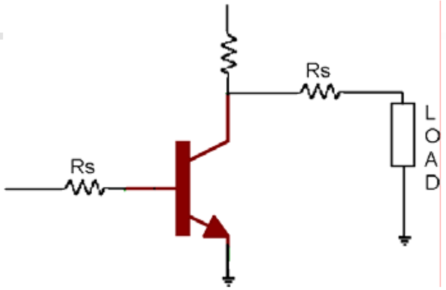


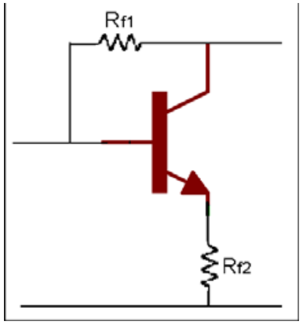

| | | |
|---|---|---|
| Load stability Circle | $S_{22} > 1$ | The area including the centre is unstable |
| | $S_{22} < 1$ | The area including the canter is stable |
| Source stability Circle | $S_{11} > 1$ | The area including the centre is unstable |
| | $S_{11} < 1$ | The area including the centre is stable |

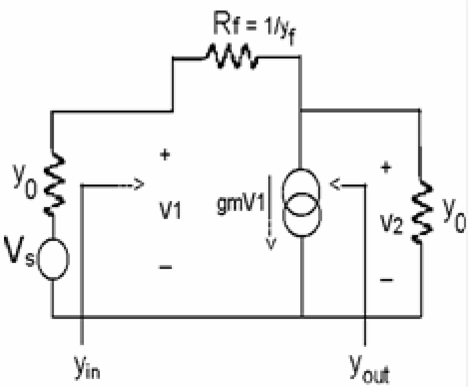
# How to make an Amplifier Stable?

- Add a resistor( Seri or Parallel)



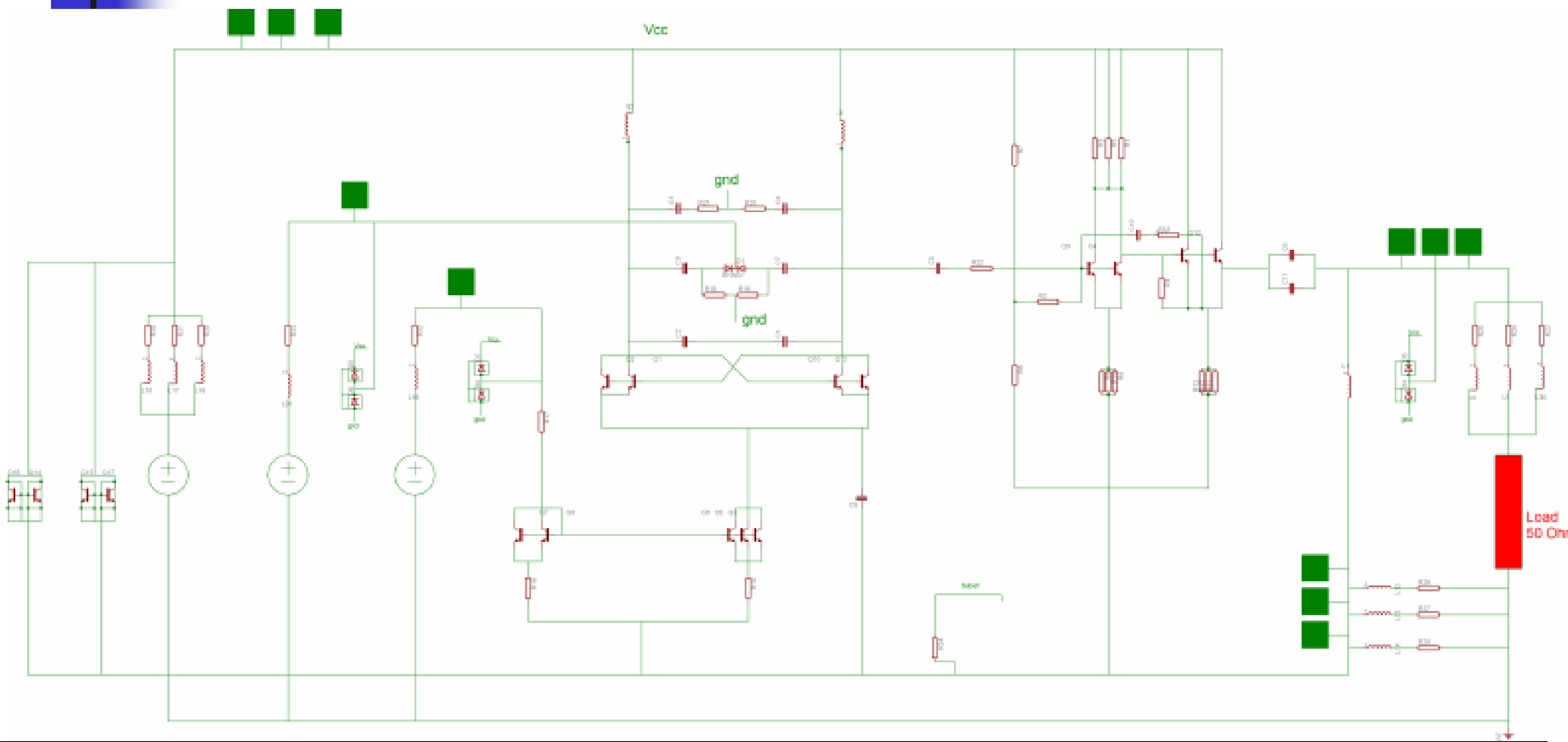

- Feed back Amplifier



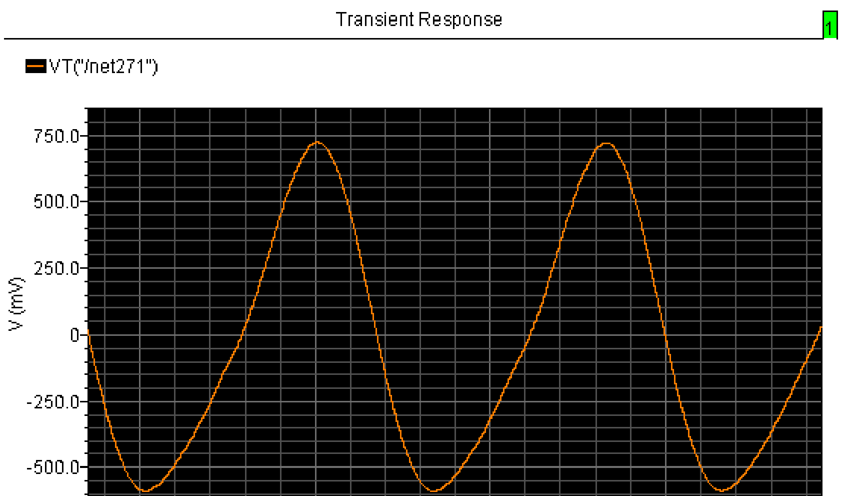




$$y_f = \frac{y_0}{1+|S_{21}|} \quad or \quad R_f = R_0(1+|S_{21}|)$$

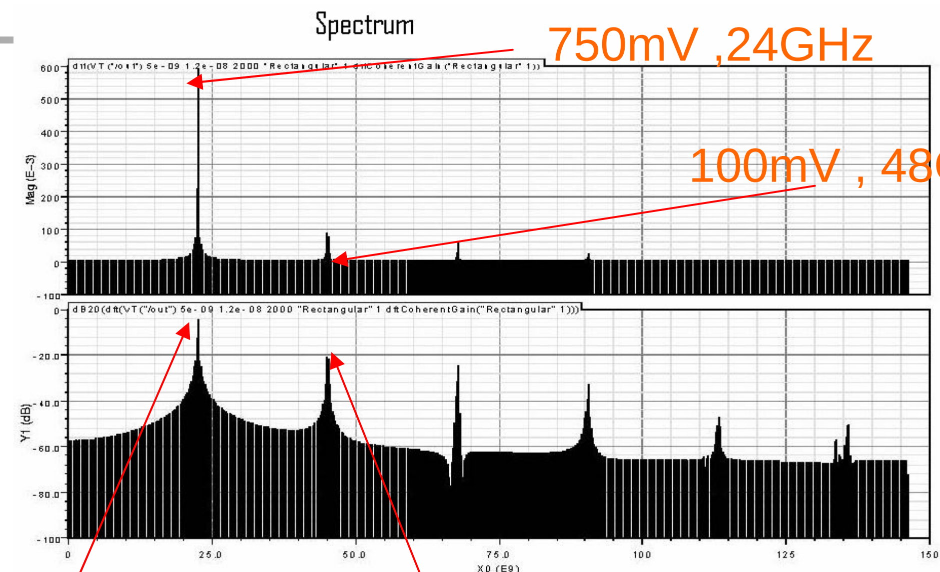
# The Complete Circuit



# Simulation Results








750mV ,24GHz

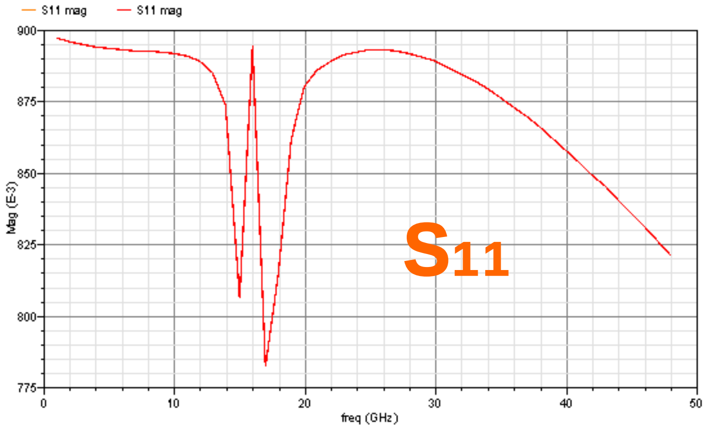
100mV , 48GHz

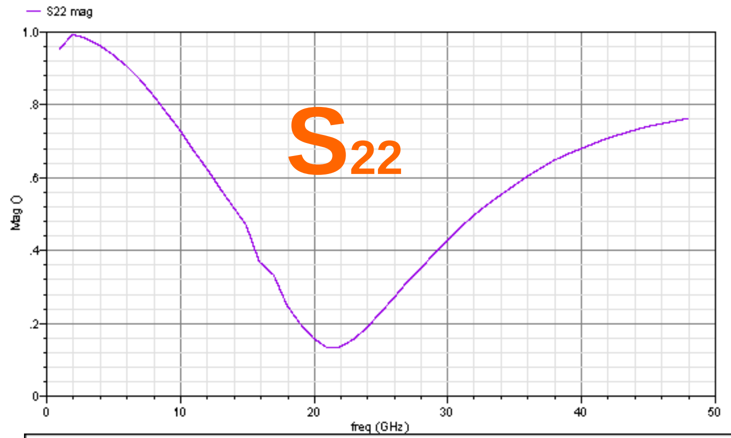
-4dB

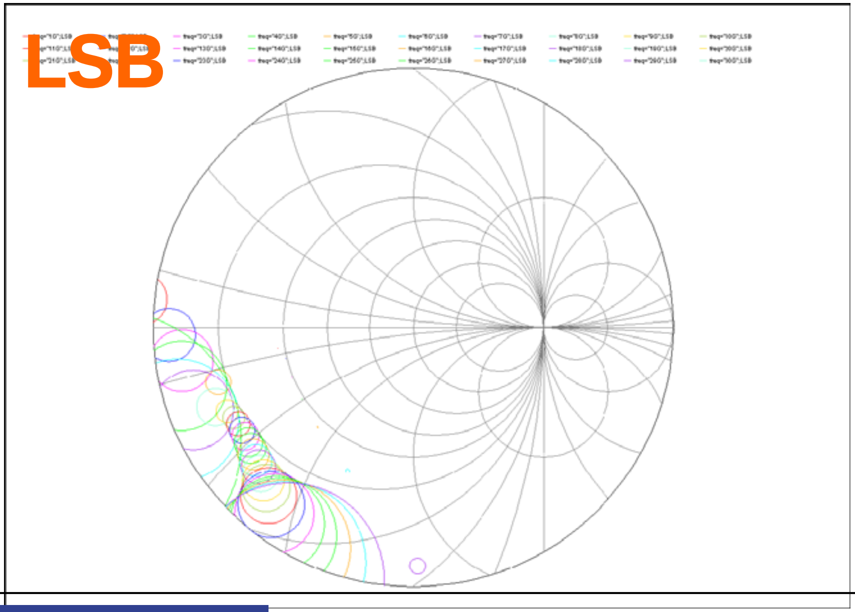
-19dB

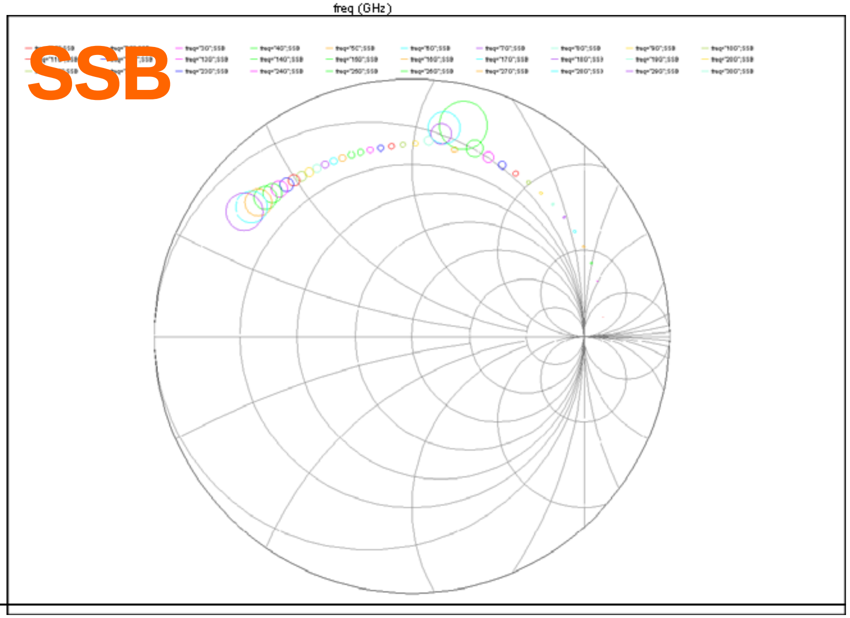
-75dBc/hz @ 100KHz

# Simulation Results

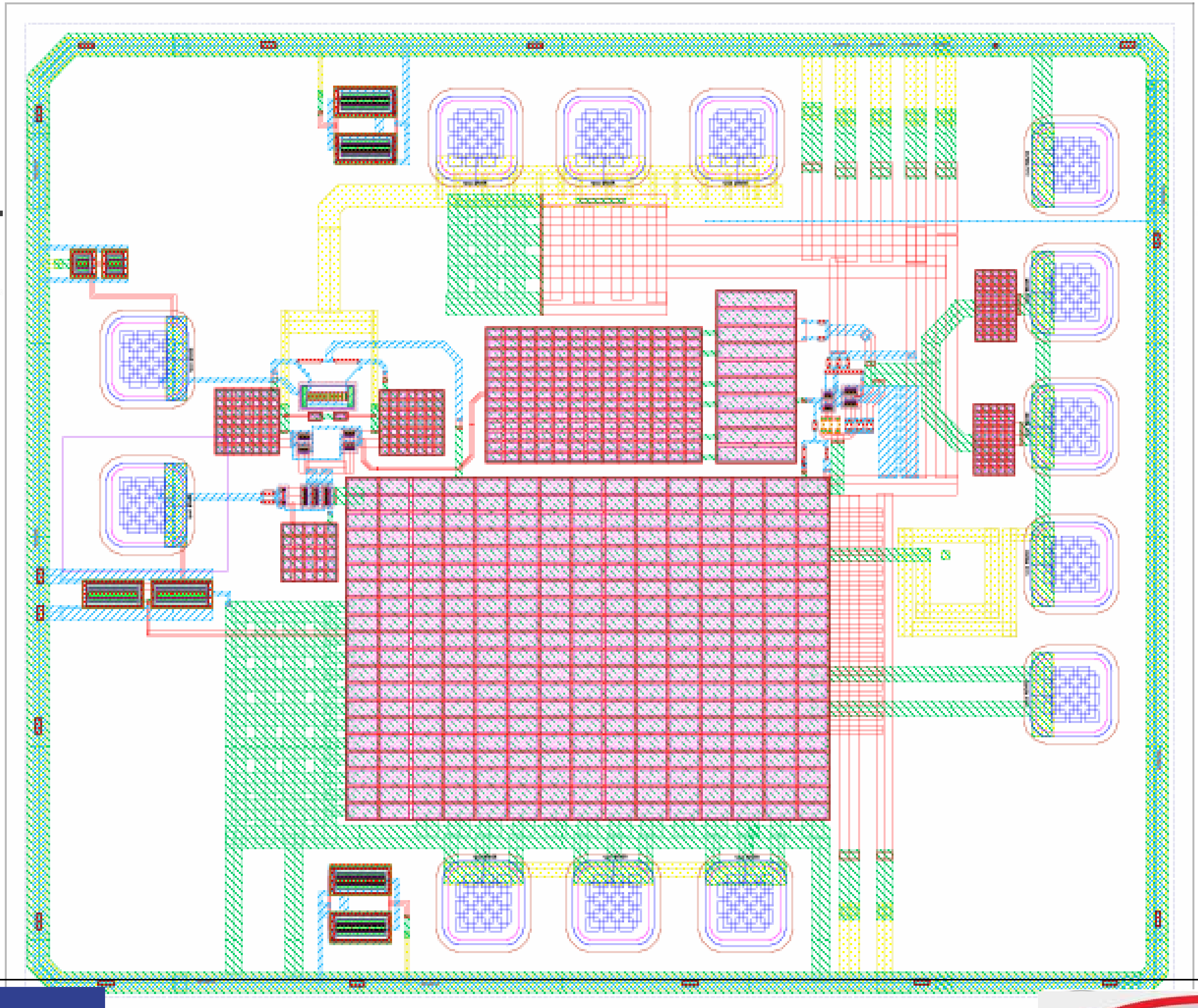


# Layout



$0.7\,mm^2$

**Symmetric**

**Parasitics Extraction**

# Thanks for the attention